

OUTLINE (V)

- MOSFETs for the ITRS in the deca-nano range
- Technological and modelling challenges according to the ITRS nodes
- Examples of modeling deca-nanometer MOSFETs



ITRS

- <http://public.itrs.net>



Table 47a High-performance Logic Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length high-performance (HP) (nm) [1]	45	37	32	28	25	22	20
EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3	1.2	1.1	1.0	0.9	0.8	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.4	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.1	2.0	1.8	1.7	1.3	1.2	1.2
Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02	1.1E+03	1.2E+03
Nominal power supply voltage (V _{dd}) (V) [6]	1.2	1.2	1.1	1.1	1.1	1.0	1.0
Saturation threshold voltage (V) [7]	0.21	0.20	0.20	0.21	0.18	0.17	0.16
Nominal high-performance NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (µA/µm) [8]	0.03	0.05	0.05	0.05	0.07	0.07	0.07
Nominal high-performance NMOS saturation drive current, I _{d,sat} (at V _{dd} , at 25°C) (mA/mm) [9]	◆ 980	1110	1090	1170	1510	1530	1590
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0	2.0	2.0
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	0.8	0.7
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R _{sd}) (Ohm-µm) [13]	◆ 180	180	180	171	162	153	144
Ideal NMOS device gate capacitance (F/µm) [14]	7.40E-16	6.39E-16	6.14E-16	5.69E-16	6.64E-16	6.33E-16	5.76E-16
Parasitic fringe/overlap capacitance (F/µm) [15]	2.40E-16	2.40E-16	2.40E-16	2.30E-16	2.20E-16	2.00E-16	1.90E-16
High-performance NMOS intrinsic delay, τ = C _{gate} * V _{dd} / I _{d,sat} (ps) [16]	◆ 1.20	0.95	0.86	0.75	0.64	0.54	0.48
Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	◆ 1.00	1.26	1.39	1.60	1.86	2.20	2.49
Nominal logic gate delay (NAND Gate) (ps) [18]	◆ 30.24	23.94	21.72	18.92	16.23	13.72	12.13
NMOSFET power-delay product (J/µm) [19]	1.41E-15	1.27E-15	1.03E-15	9.66E-16	1.07E-15	8.33E-16	7.66E-16
NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	3.96E-07	6.60E-07	6.05E-07	6.05E-07	8.47E-07	7.70E-07	7.70E-07

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



The Power crisis



On track with the roadmap

- Scaling the traditional MOS at and below the 65nm node exacerbates several well-known challenges: SCE control, Ion/Ioff, gate leakage, etc, because of the many non-scaling factors
- $EOT < 1 \text{ nm}$ and $N_d > 10^{18} \text{ cm}^{-3}$ necessary to meet the ITRS requirements for bulk MOS
- Alternative structures (e.g. DG-UT-SOI) and materials (high k, metal gate, high-mobility channel materials) will be required to continue scaling.
- Innovative structures require physically-based device simulations.



The ITRS Scenario

- The 65 nm technology node requires the introduction of strained channel material to boost mobility.
- At 45 and 32 nm TN, MOS architecture may require substantial modifications by the introduction of Ultra-Thin silicon, possibly strained, SOI MOSFET, in order to meet SCE requirements (I_{ON} / I_{OFF}).
- The I_{ON} of MOSFETs is limited by mobility when scattering dominates transport and to a maximum current I_{BL} in the limiting case of ballistic transport
- Increase of I_{ON} demands:
 - Increase of mobility
 - Increase of Ballistic Ratio $BR = (I_{ON} / I_{BL})$ (Technology Booster in the ITRS Roadmap)
 - Increase of maximum current I_{BL} (material)

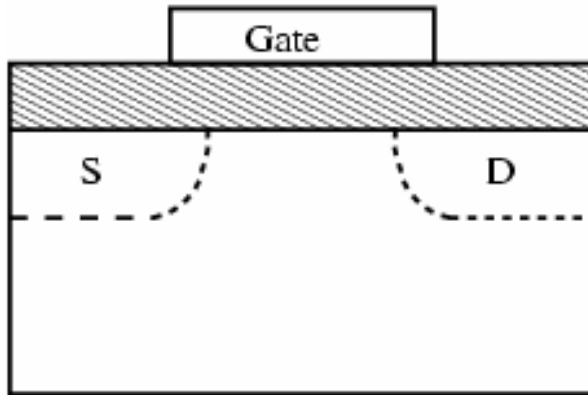


Double Gate (or Multigate) MOSFETs on Ultra Thin Silicon Films (I)

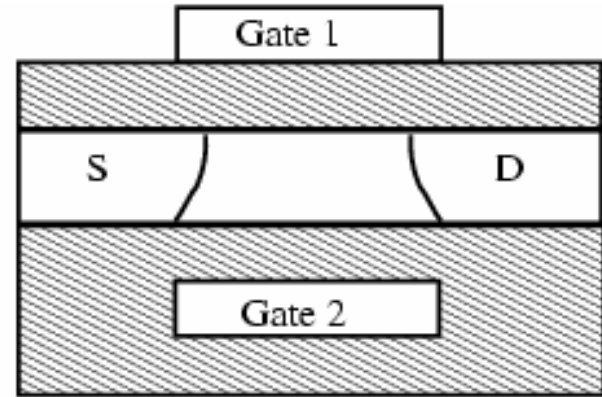
- Relax [L_G /EOT] constraint to preserve electrostatic integrity (I_{OFF})
- Virtually Undoped Si Films $\Rightarrow \mu_{eff} \uparrow \uparrow$,
decreases capacitance, prevents
statistical doping fluctuation



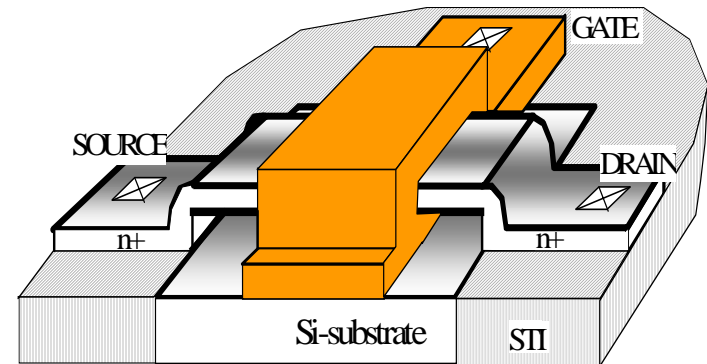
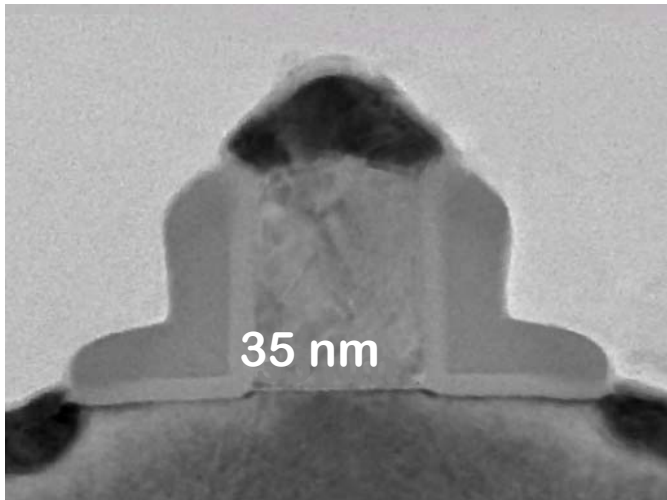
Bulk vs. SOI



Conventional Bulk MOSFET

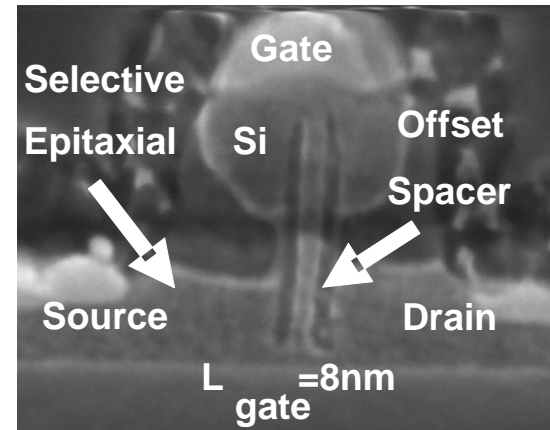
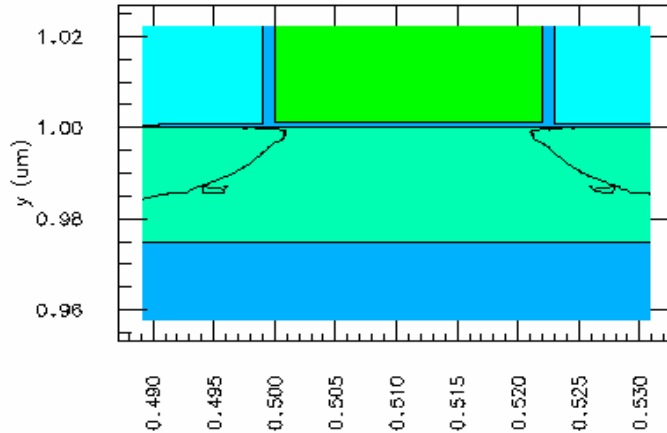


Double gate MOSFET

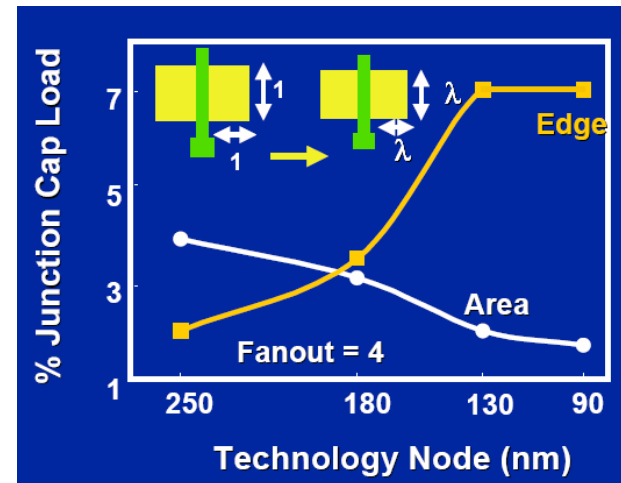


Ultra-thin SOI

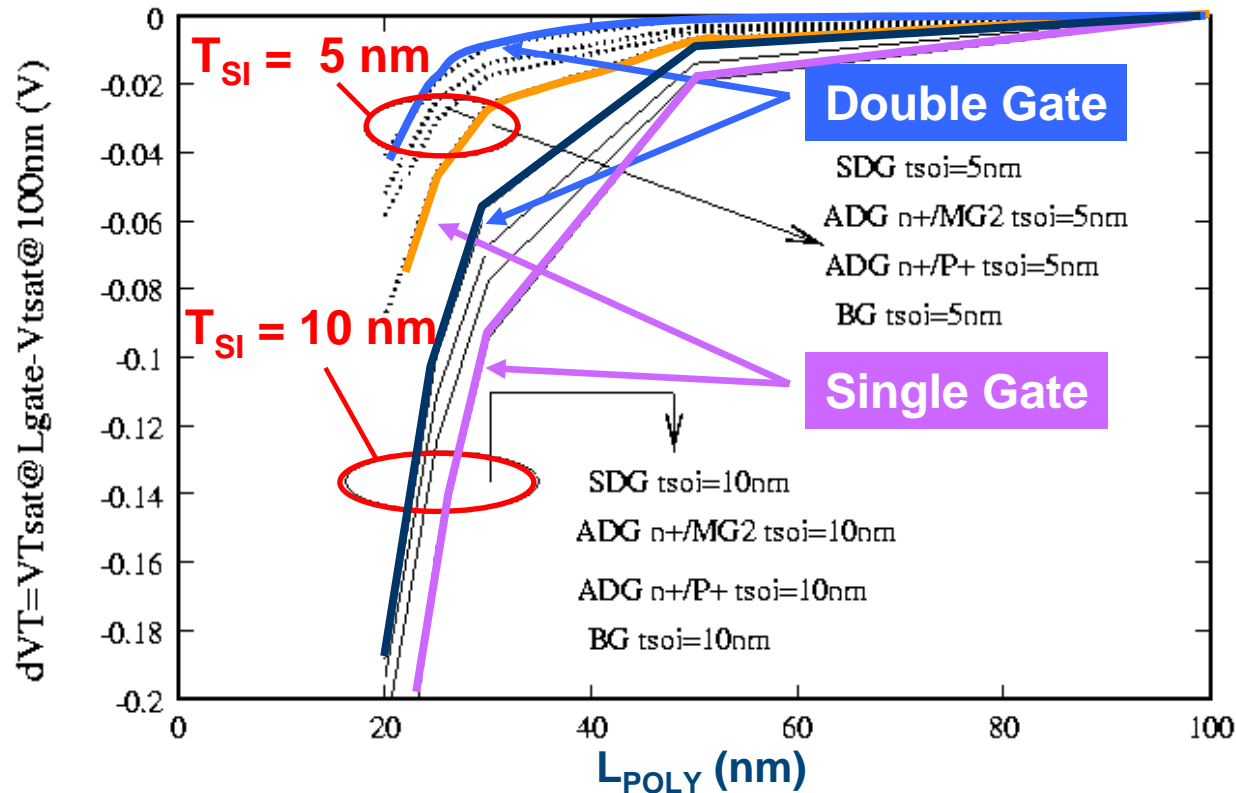
$t_{Si} = 25 \text{ nm}$



- 15-20% delay reduction at the same off current
- Cause:
 - Perimeter C_j reduction
 - Improvement in SCE



Double Gate Scaling Advantages



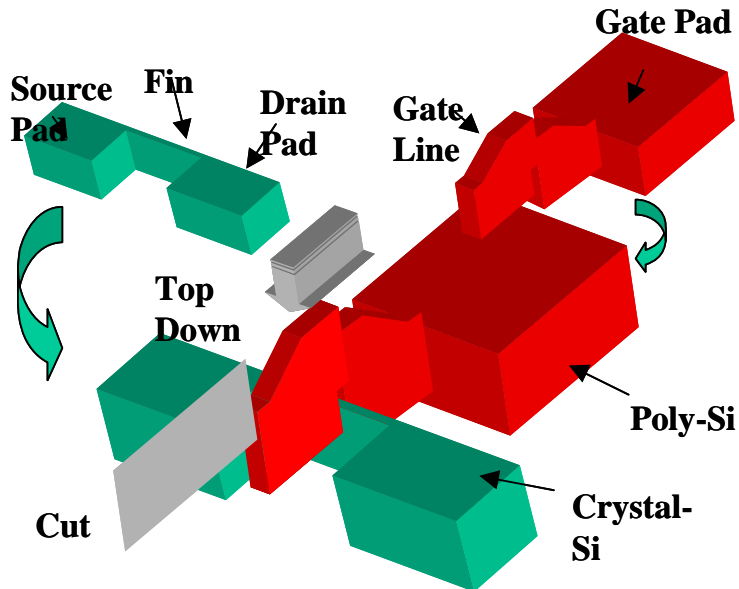
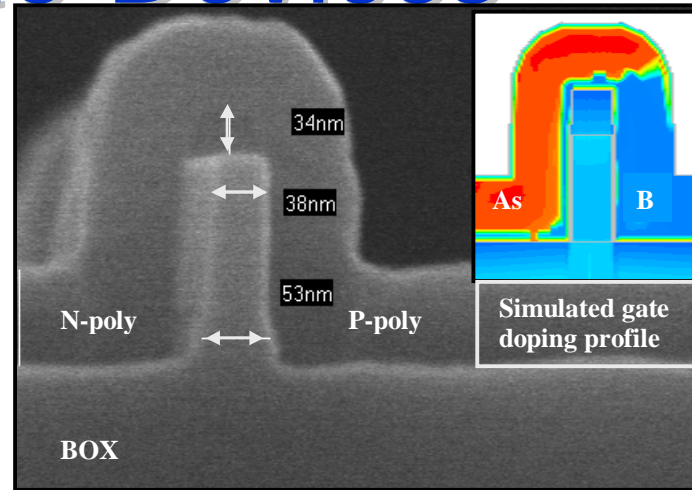
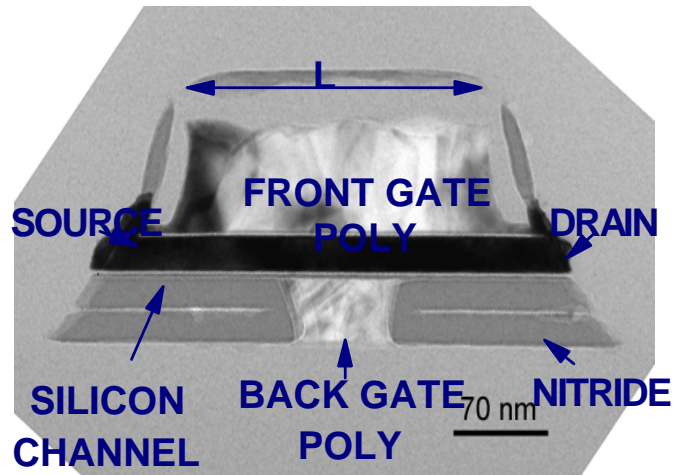
SDG = Symmetric Double Gate

ADG = Asymmetric Double Gate

BG = Back Gate: Single gate operation

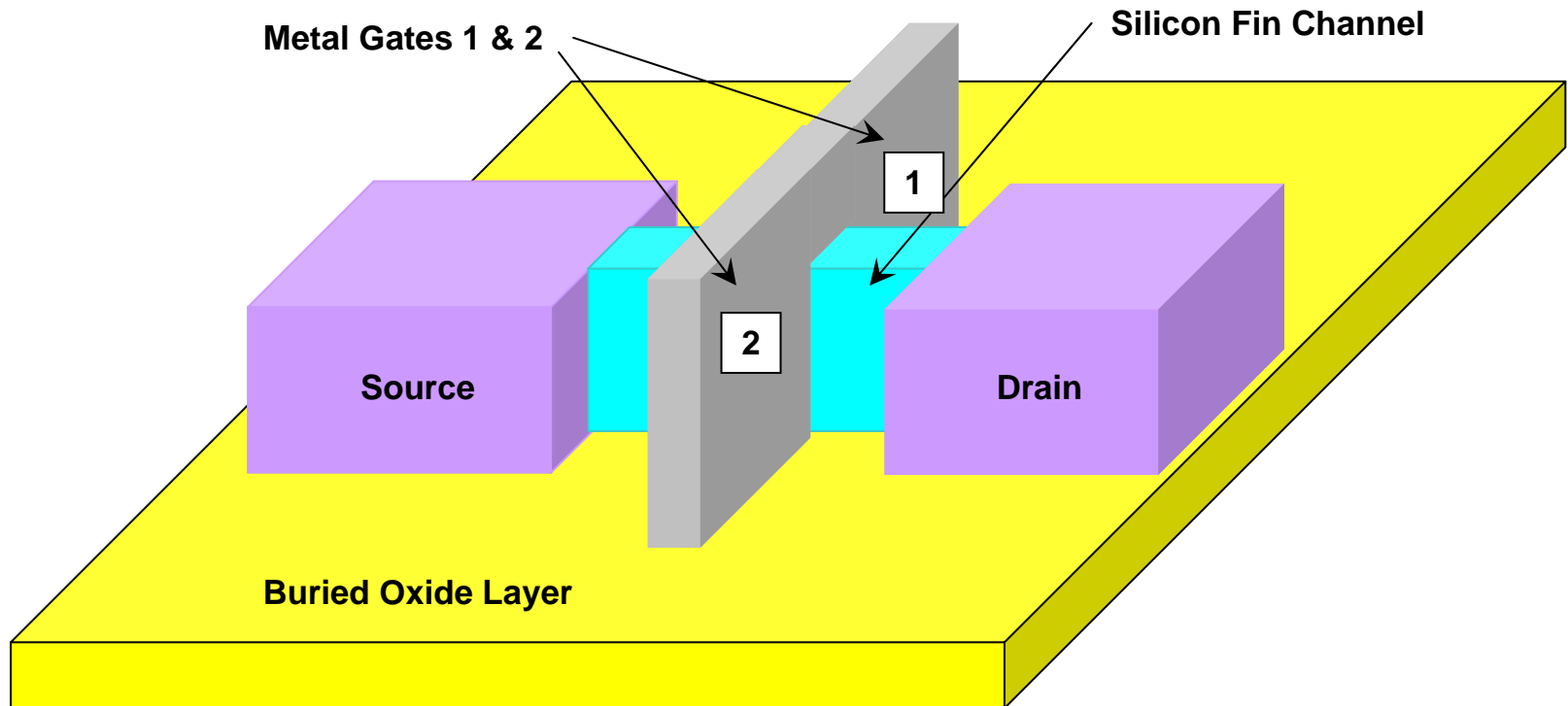


Double Gate Devices



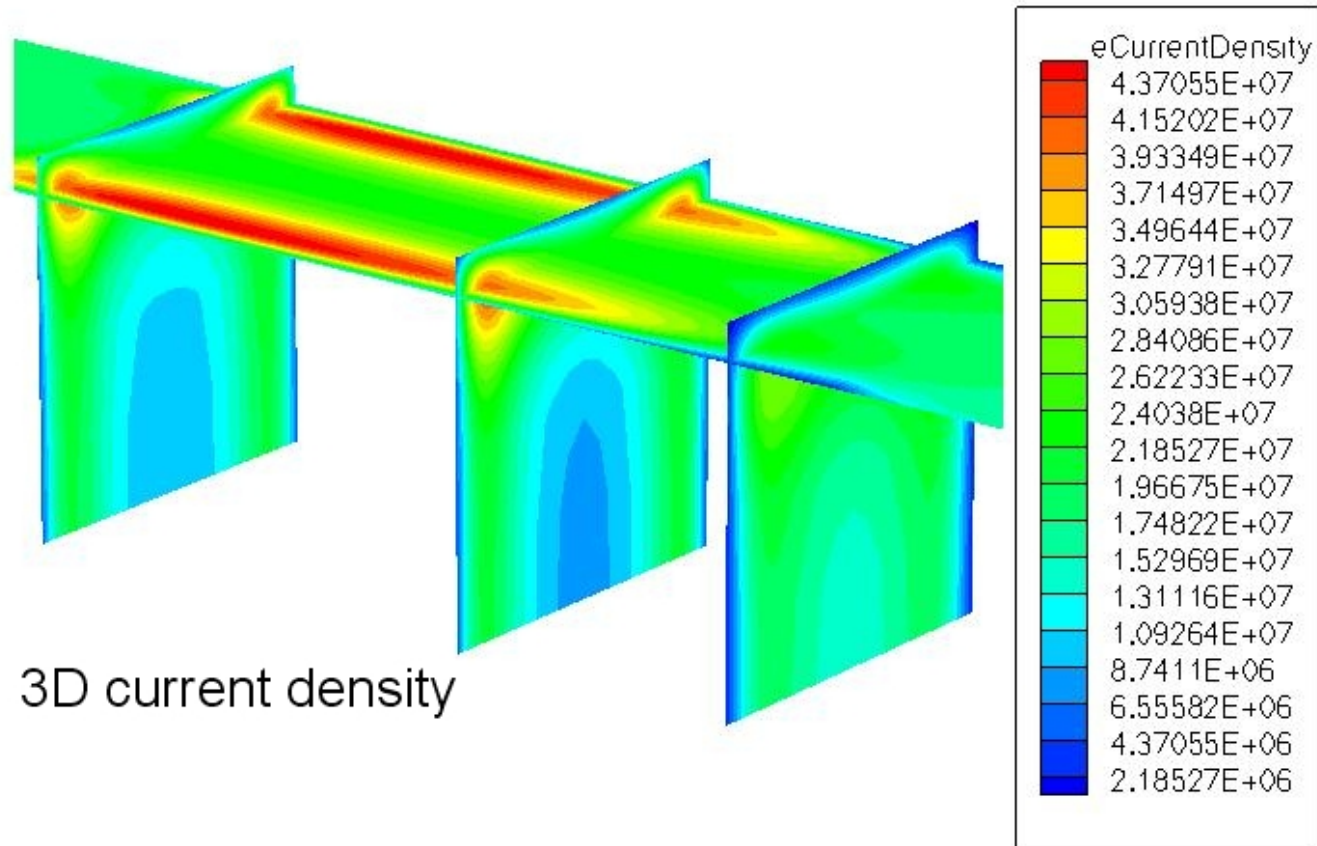
Multigate - FINFET

Surrounded gate suppress the leakage between S and D

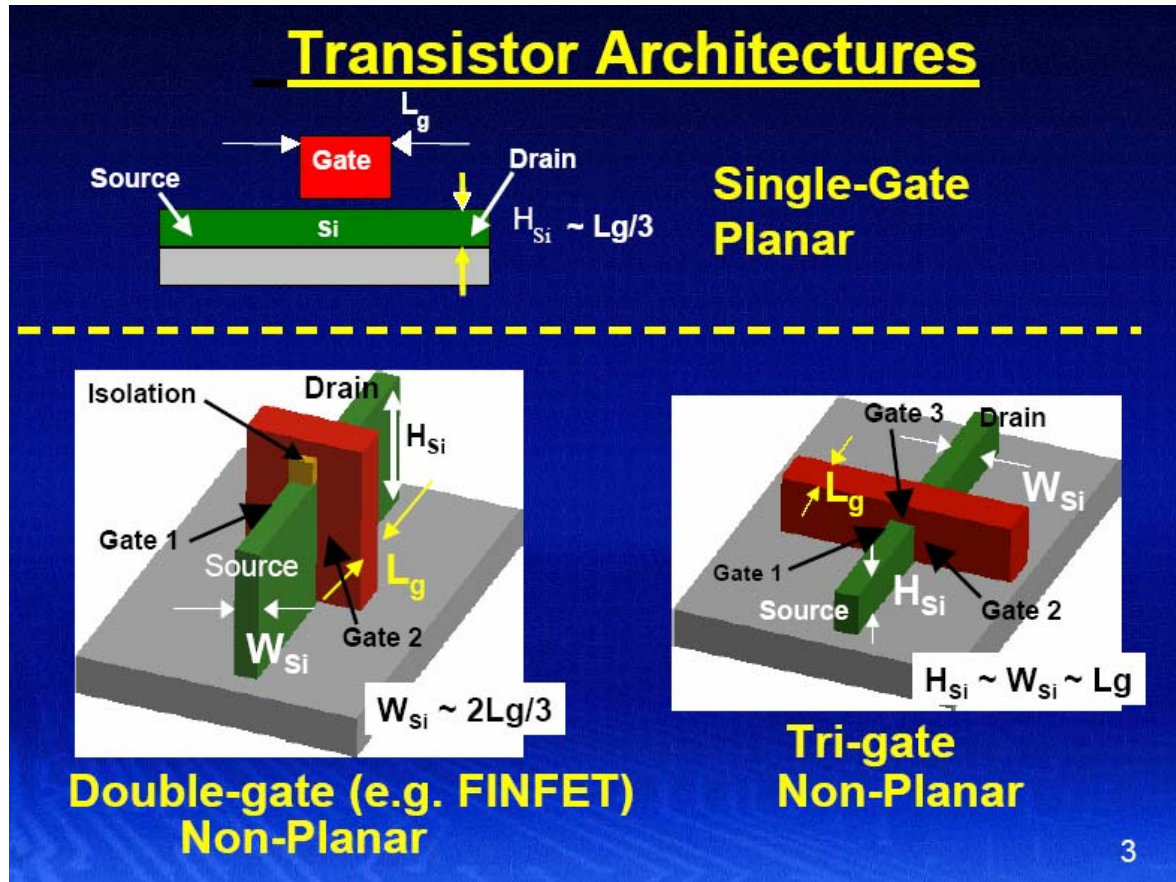


-  = High N doping
-  = Light P doping

FinFET is a real 3D device



Tri-Gate



Intel: VLSI 2003

- Worse SCE due to lower effective doping at the edge

FinFET Pro's and Con's

- High current drivability
- 3-D integration
- Still many different solutions under investigation
- Technological challenges
- Design issues (substrate contact)

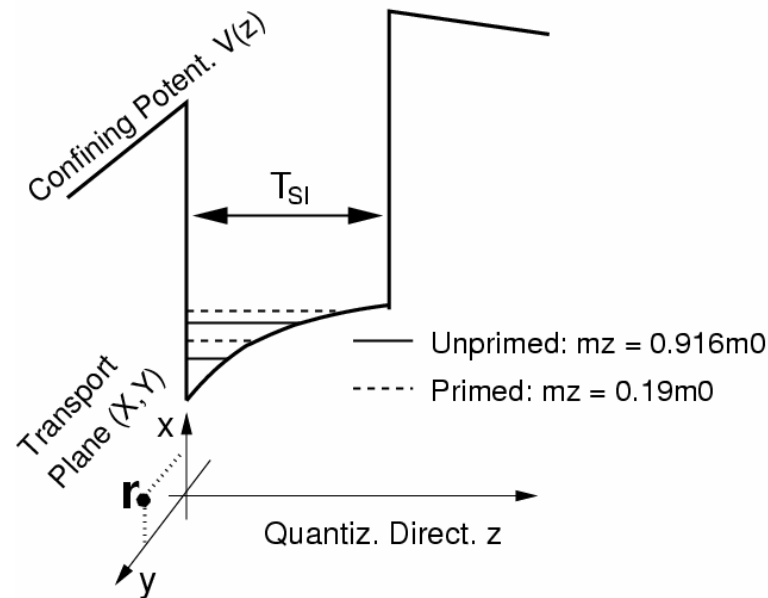


Relevant issues in deca-nano MOSFETs

- (I) Quantum confinement (channel confinement)
- (II) Quantum penetration (Leakage through the gate)
- (III) Improved mobility by channel material engineering
- (IV) Lateral transport is semi-ballistic (?) and influenced by quantization

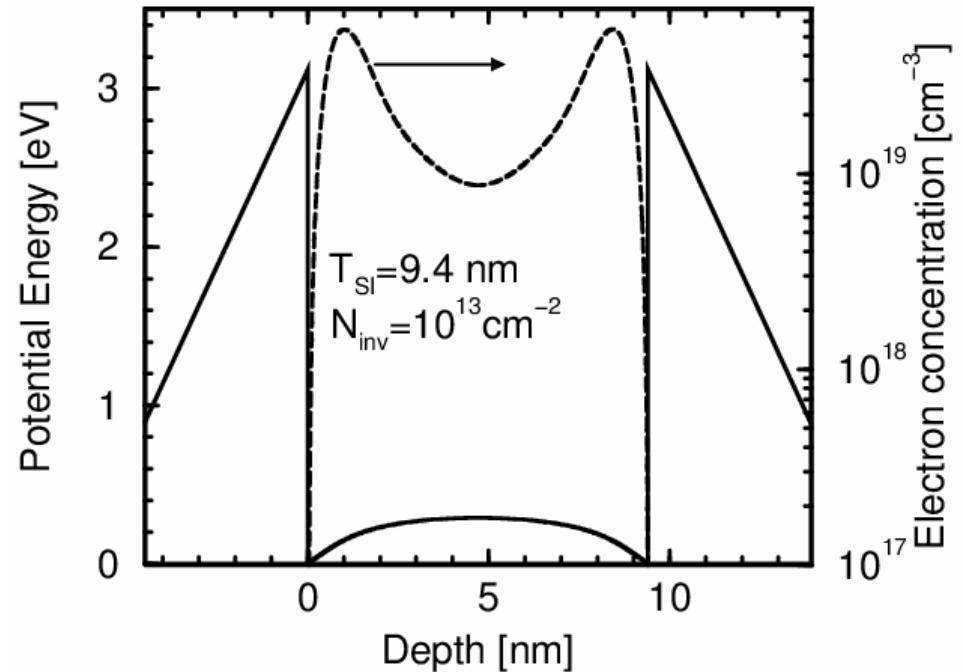
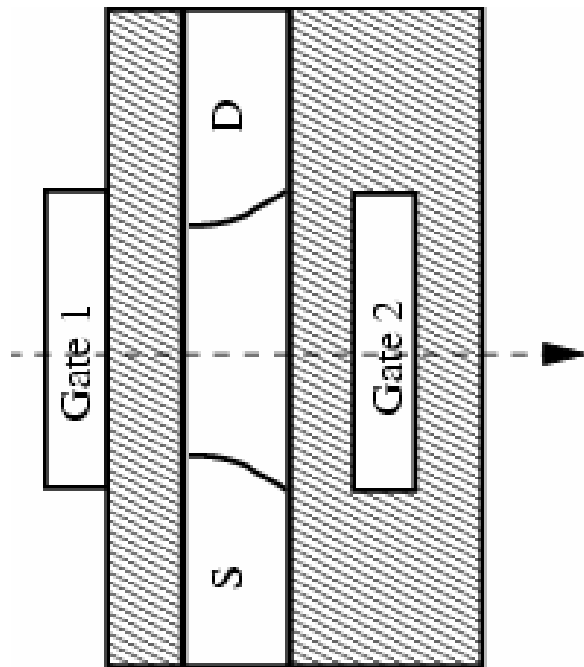


Channel acts as a quantum well: vertical quantum confinement in the inversion well

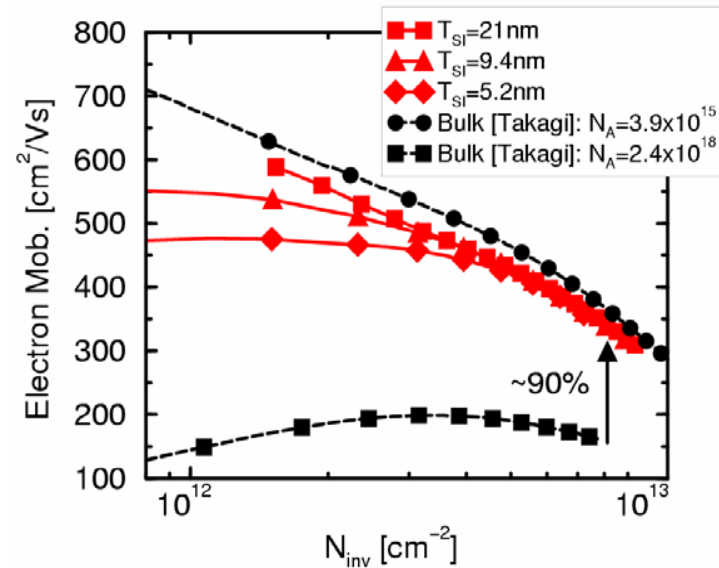
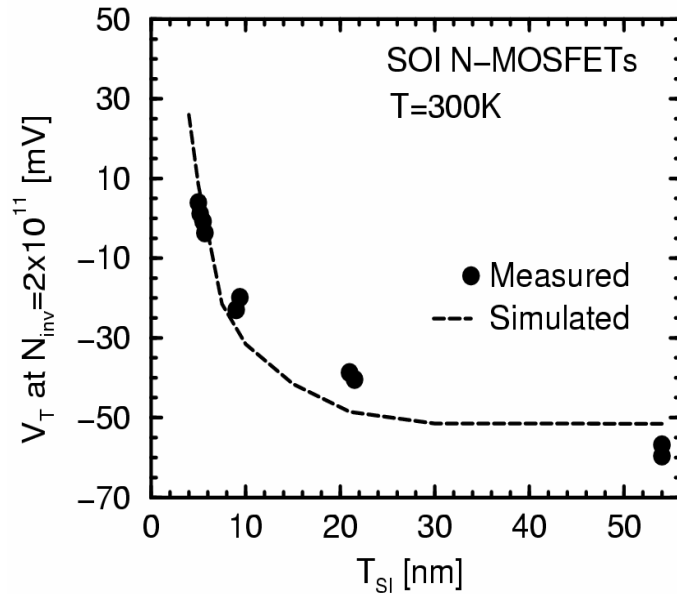


- $\mathbf{r} = (x, y)$ $\mathbf{k} = (k_x, k_y)$: in Plane Position and Wavector
- Silicon 6 Minima yield Two Sets of Subbands

Electrostatic of the device is strongly affected by quantum confinement



Effects of Vertical Quantization in MOSFETs



Size Induced Quantization affects:

- Eigenvalues and Electrostatics: Thresh. Voltage
- Scattering Rates: Low Field Effective Mobility (μ_{eff})

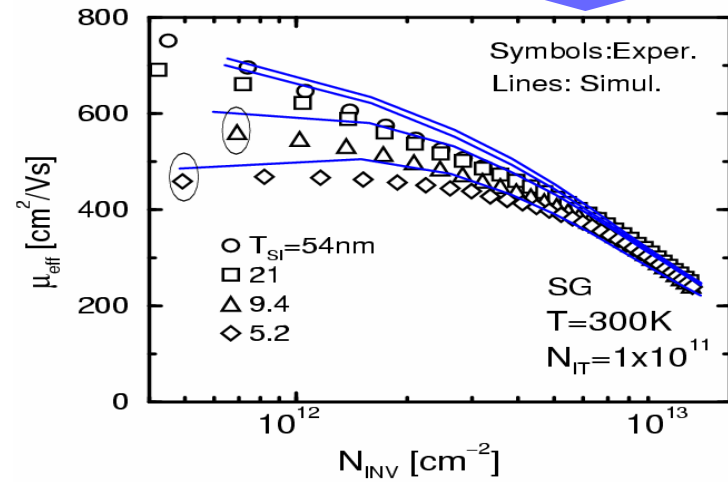
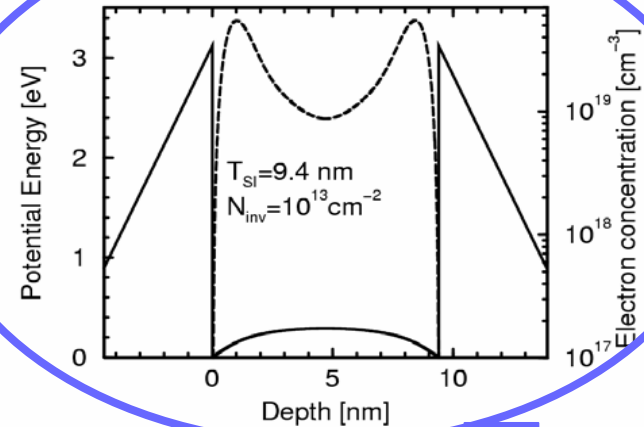
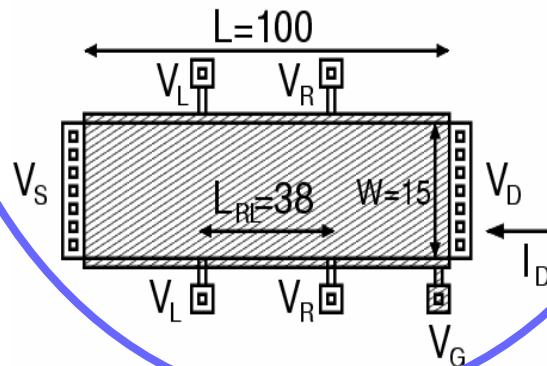
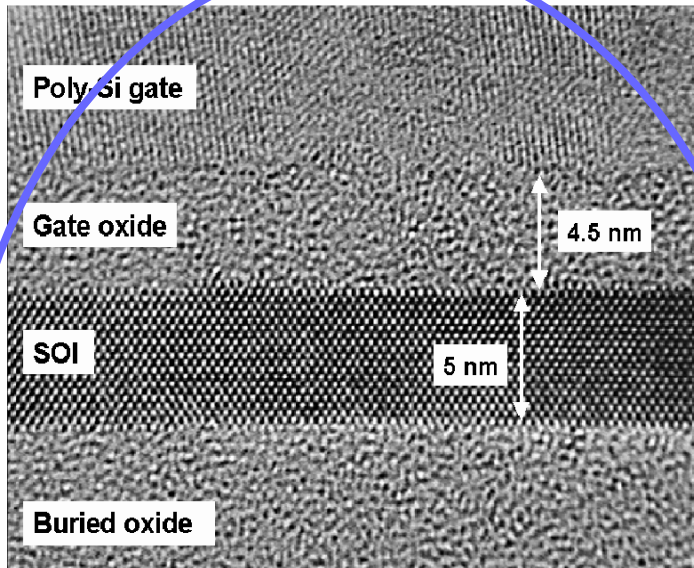
Effects of Vertical Quantization in MOSFETs

Low-field Mobility in Ultra-thin SOI:

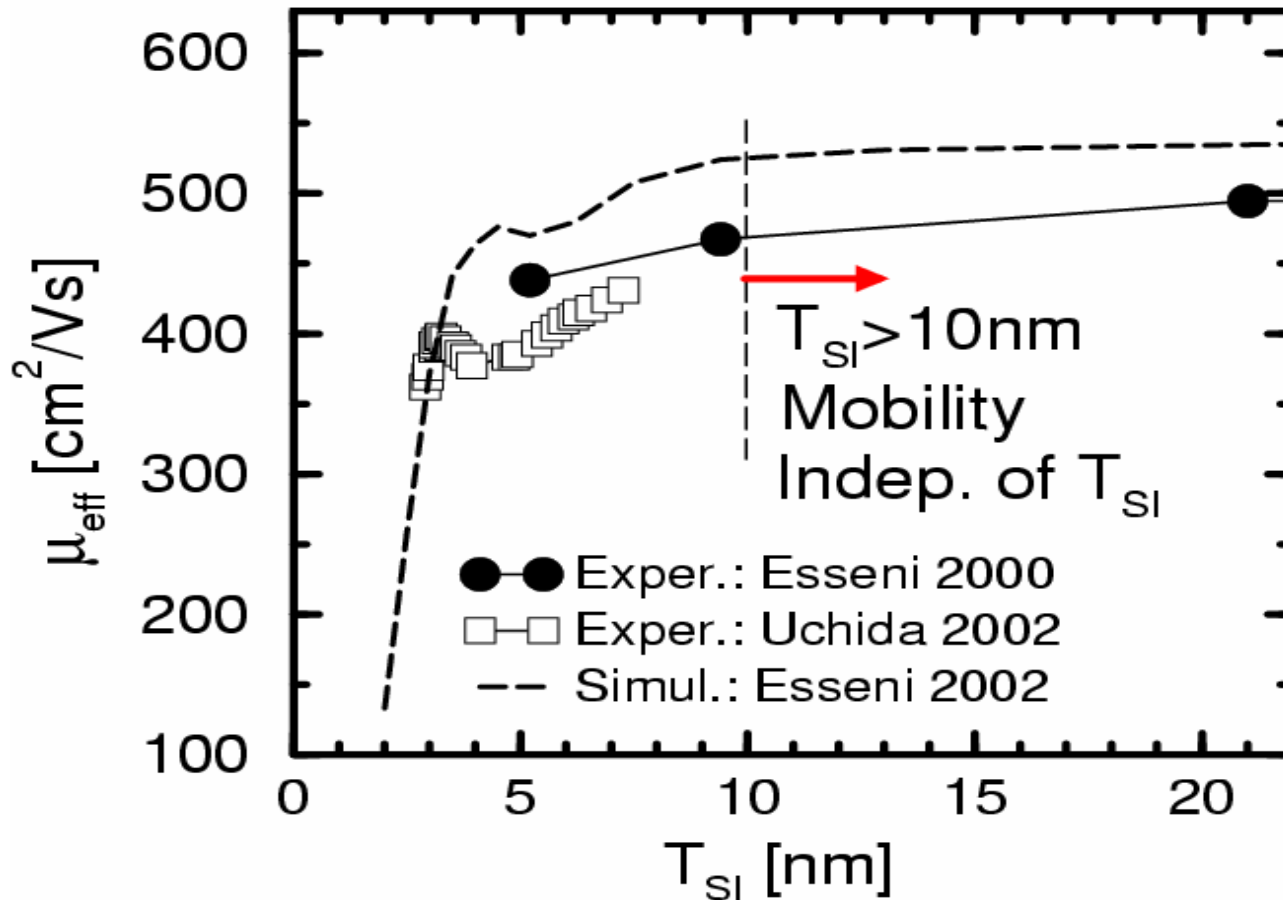
- Modeled via Momentum Relaxation Time (MRT): approximated solution of the BTE assuming the distribution functions in each sub-band $f_i(k)$ are Displaced Maxwellians



Low-field Mobility in Ultra-thin SOI



Low-field Mobility in Ultra-thin SOI



Relevant issues in deca-nano MOSFETs

- (I) Quantum confinement (channel confinement)
- (II) Quantum penetration (Leakage through the gate)
- (III) Improved mobility by channel material engineering
- (IV) Lateral transport is semi-ballistic (?) and influenced by quantization

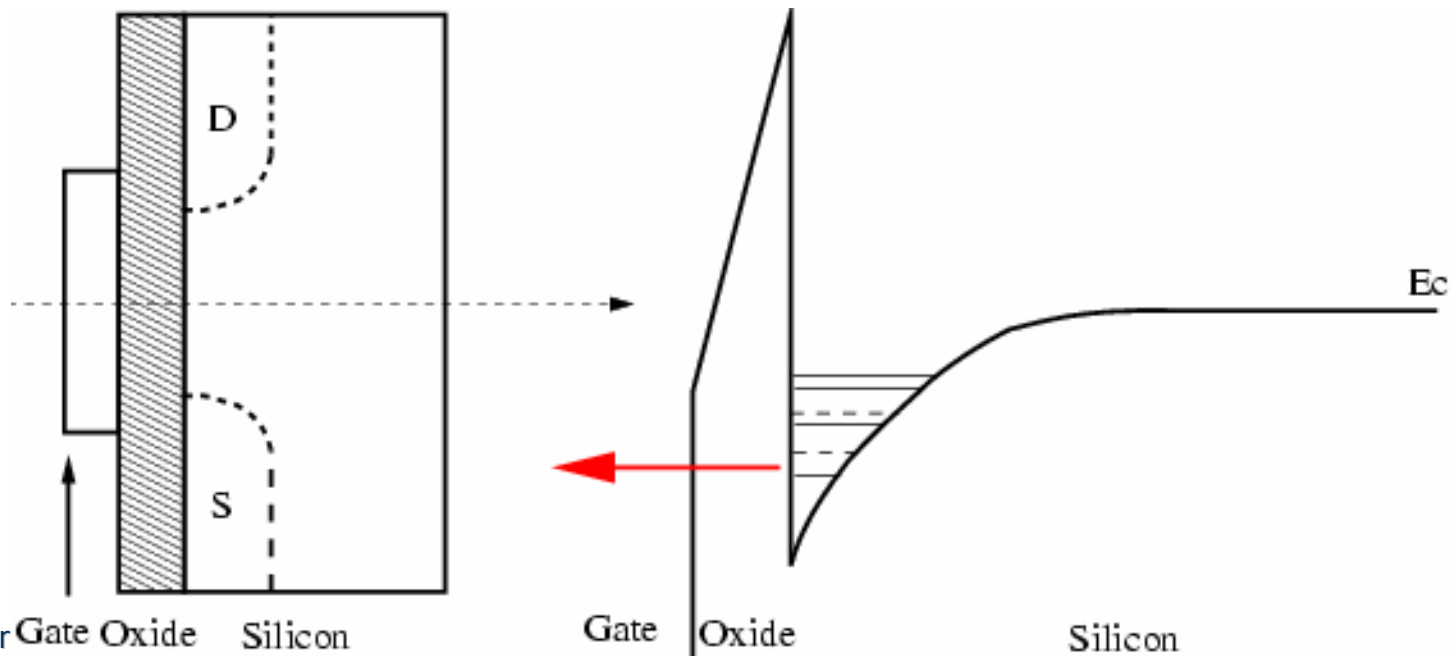


Relevant Simulation Issues for Decanano-MOSFETs simulation

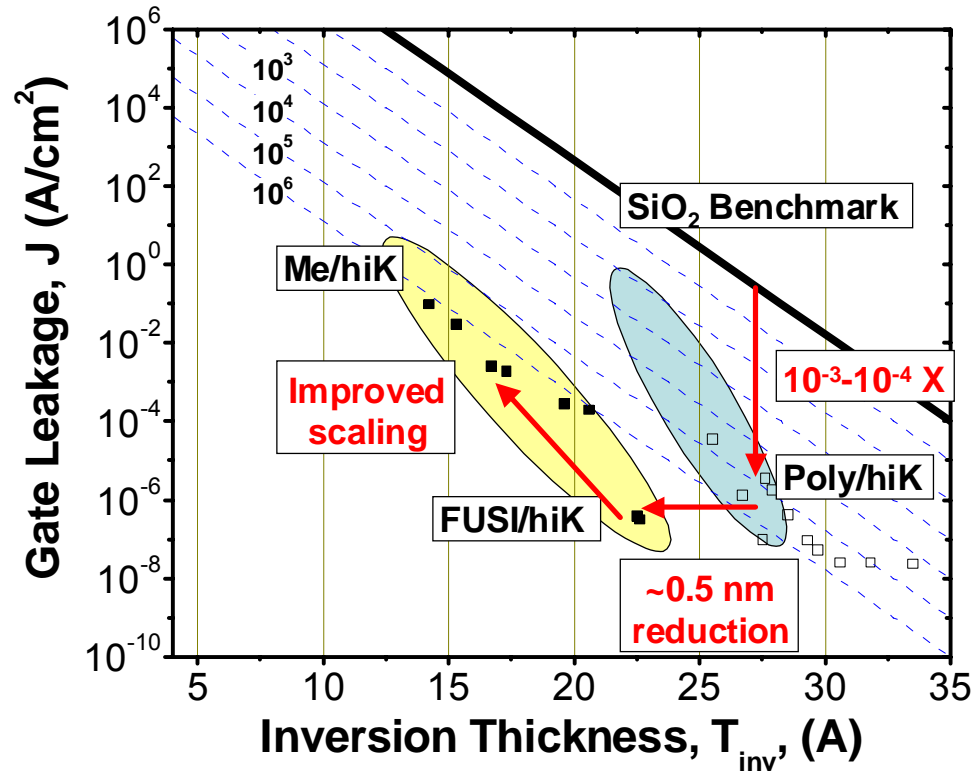
Gate oxide thickness scaling below 2 nm causes **relevant direct tunneling current**

Polysilicon depletion sums-up to unacceptable EOT

Solution: high-k insulator and metal gate



Metal Gate - High K



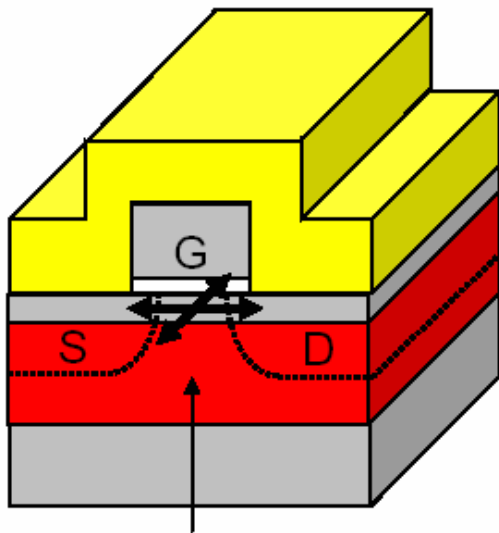
- Promise: Lower T_{inv}
 - ~20% drop in T_{inv} will result in 10% frequency gain
- Metal has to be band edge

Relevant issues in deca-nano MOSFETs

- (I) Quantum confinement (channel confinement)
- (II) Quantum penetration (Leakage through the gate)
- (III) **Improved mobility by channel material engineering**
- (IV) Lateral transport is semi-ballistic (?) and influenced by quantization

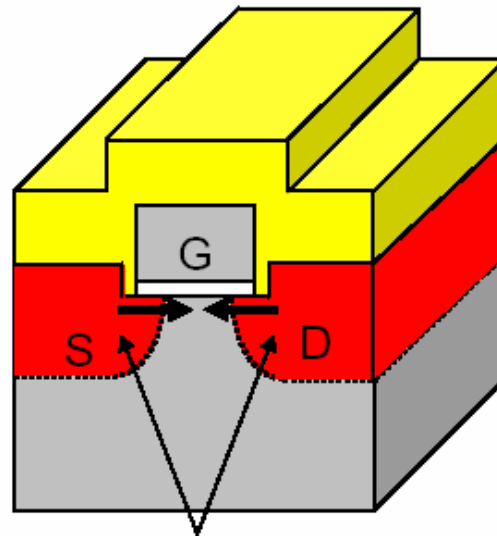


Mobility Enhancement: Strained Silicon



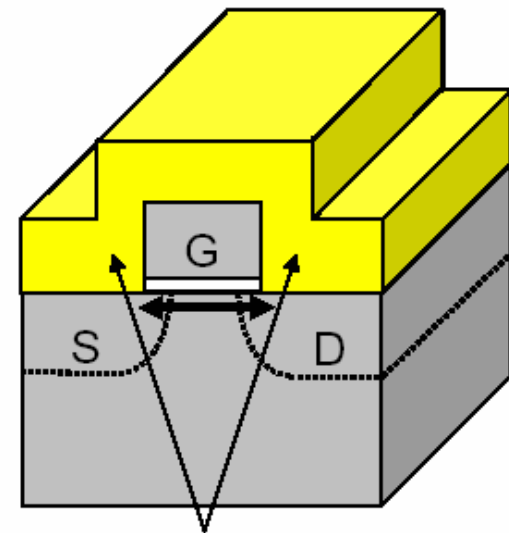
Graded SiGe Layer

Biaxial
Tensile Strain



Selective SiGe S-D

Uniaxial
Compressive Strain
for PMOS

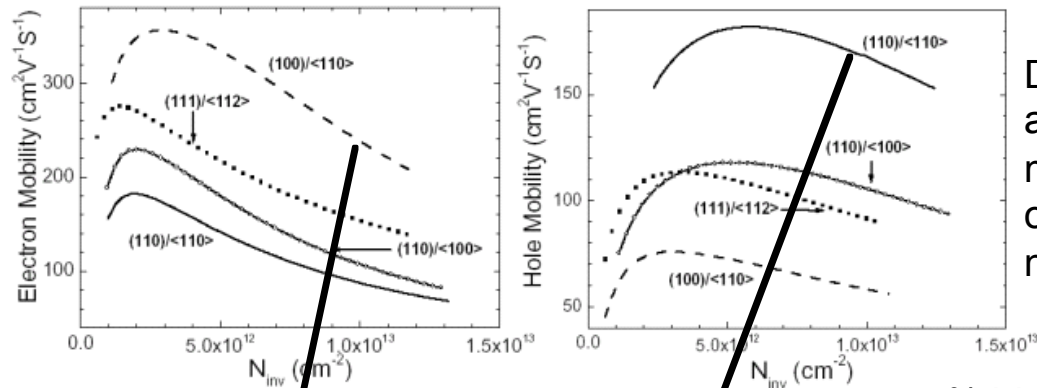


Tensile Si₃N₄ Cap

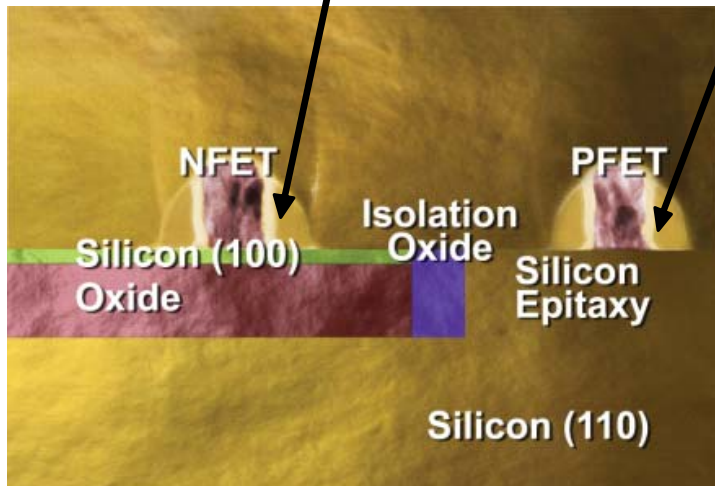
Uniaxial
Tensile Strain
for NMOS



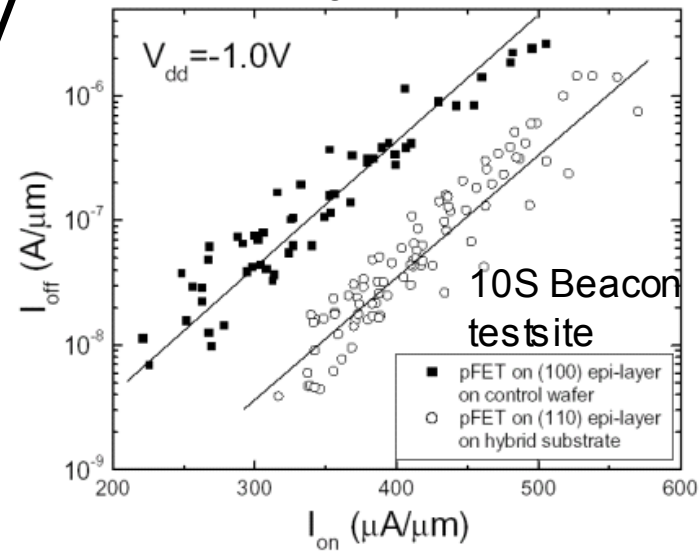
Transport on 110 Surface



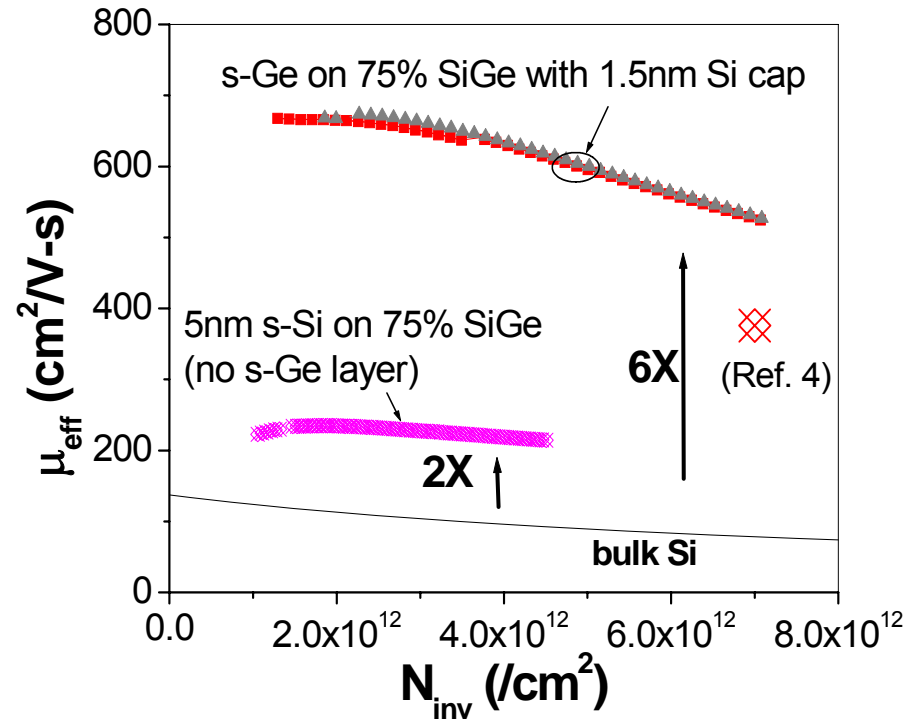
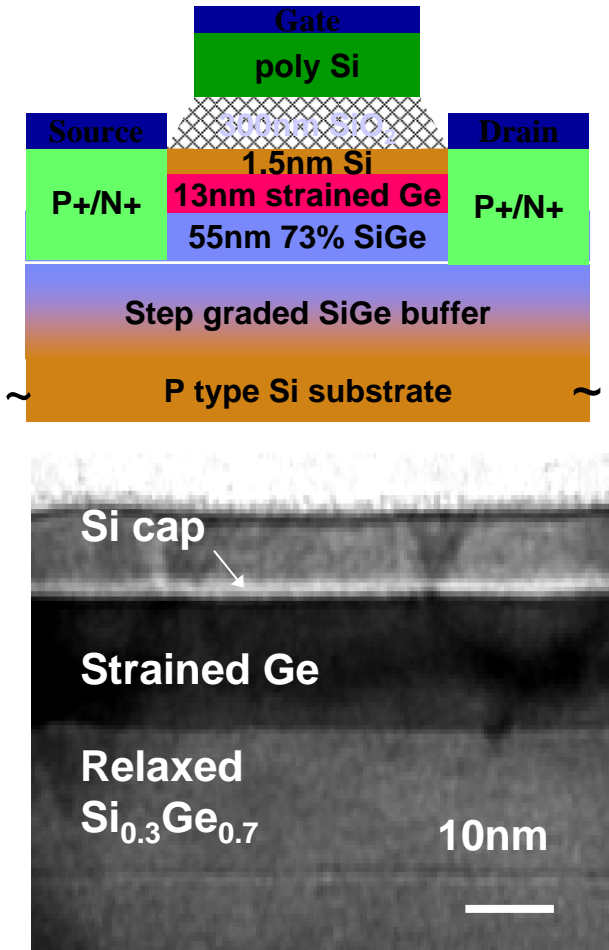
Developed substrate and processes of high mobility surface orientation for both nFETs & pFETs



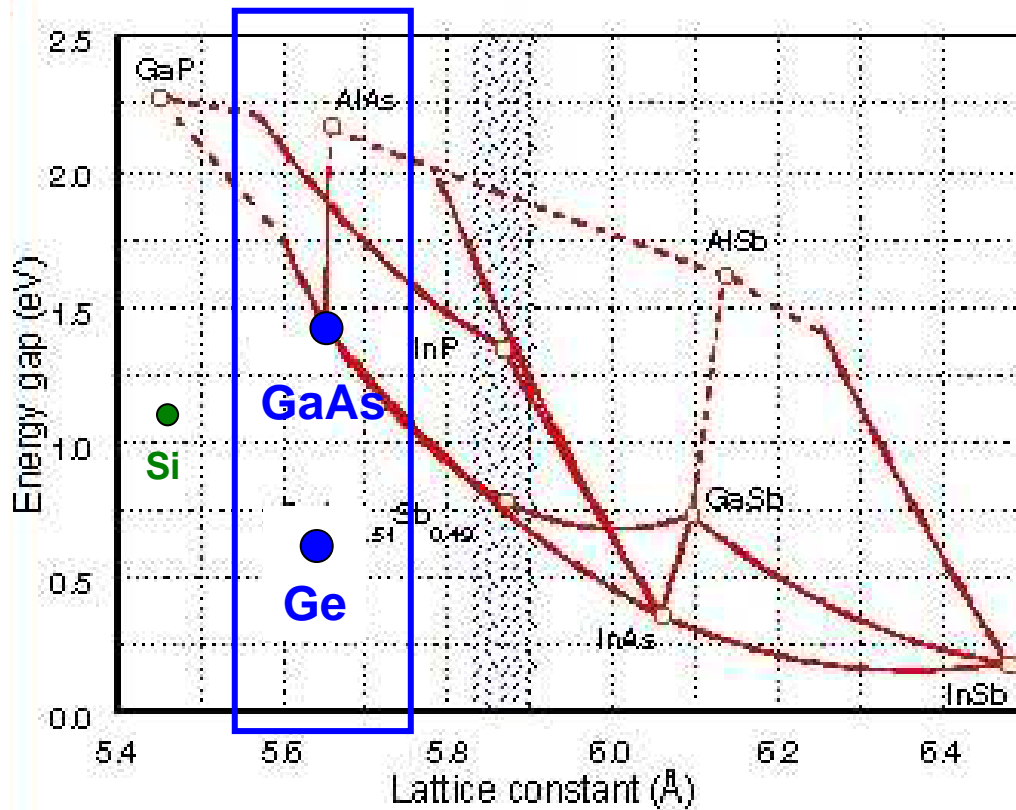
~35 % higher pFET I_{dsat}



Strained Ge



III-V Integration with Germanium



Material	μ_e (cm^2/Vs)	μ_h (cm^2/Vs)
Diamond	2200	1800
Si	1350	480
Ge	3900	1900
InP	5400	200
GaAs	8500	400
InGaAs (53%)	12000	300
InAs	40000	500
GaSb	3000	1000
InSb	77000	850

- GaAs + Ge could provide optimal electron/hole mobility combination.

Relevant issues in deca-nano MOSFETs

- (I) Quantum confinement (channel confinement)
- (II) Quantum penetration (Leakage through the gate)
- (III) Improved mobility by channel material engineering
- (IV) Lateral transport is semi-ballistic (?) and influenced by quantization



The Modeling Approach

- Modeling I_{ON} at $L_G < 25\text{nm}$ requires:
 - Carrier quantization (2D Electron gas)
 - Non-equilibrium transport
 - Inclusion of complex scattering mechanisms
- Approaches:
 - Multi sub-band Monte Carlo for 2D electron gas
 - 3-D Monte-Carlo with quantum corrections (valid only if carrier confinement does not affects transport, i.e. $T_{si} \geq 10\text{ nm}$)



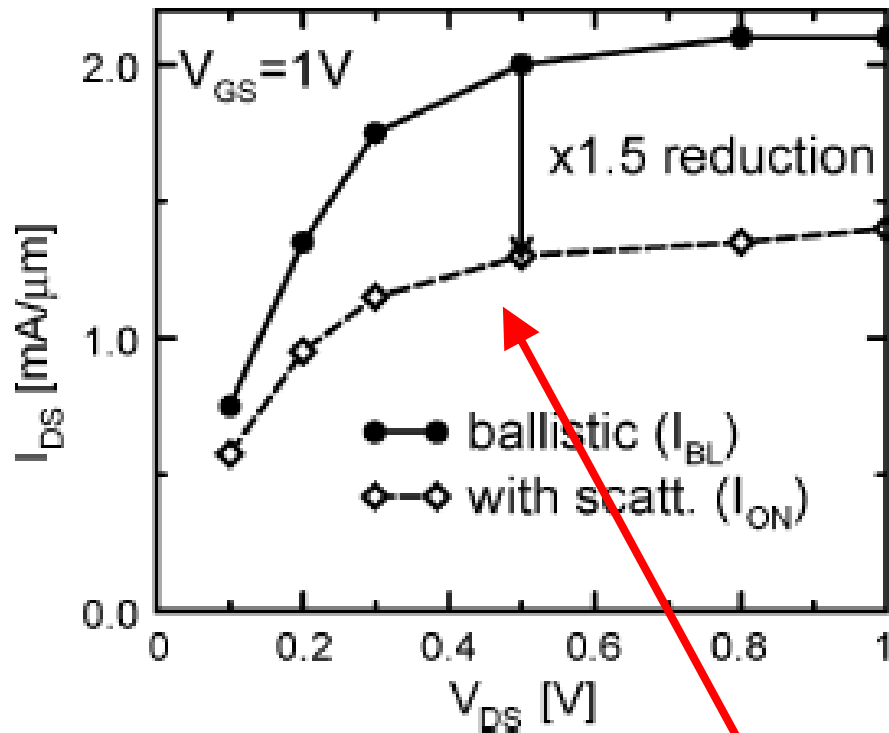
Design of the ITRS Devices

- Four Technology Nodes (TN):
 - Bulk MOSFETs: 130nm, 90nm and 65nm
 - DG SOI MOSFETs: 90nm, 65nm and 45nm
- Used ITRS Roadmap of HP Logic Devices for:
 - Supply Voltage V_{DD}
 - Equivalent Oxide Thickness EOT_{EQ} ($\epsilon_{ox}=7$)
 - Nominal L_G for each Technology Node
 - Depth of Contact junctions and S/D Extensions as well as Lateral Abruptness
- Tailoring of Channel Doping (Bulk) and T_{SI} (DG-SOI): $DIBL \sim 100$ [mV/V] at the nominal L_G
- Approx. same V_T for Bulk and SOI: Gate Work function engineering in DG-SOI
- Double Gate SOI: Electrical Integrity achieved with $T_{SI} \geq 10$ nm
- Metal Gates and very small R_{SR}
- Conservative values of $I_{OFF} < 60$ [nA/mm]

Parameters of the simulated devices

Technology Node (nm)		130	90	65	45
Supply Vol. Vdd(V)		1.2	1.2	1.0	1.0
Nominal Gate Length (nm)		65	37	25	18
Relative Dielectric Const.		7	7	7	7
Tox/EOT (nm)		2.87 /1.6	2.15 /1.2	1.6/0.9	1.26/0.7
DGSOI	Tsi (nm)		17	12	10
	DIBL (mV/V)		109	107	112
	Ioff (nA/μm)		4	7	10
	Gate WF(eV)		4.6	4.6	4.6
BULK	Nsub(10^{18} cm^{-3})	2.5	2 + halo	3+ halo	
	DIBL (mV/V)	126	130	132	
	Ioff (nA/μm)	2.5	30	60	
	Gate WF(eV)	4.05	4.05	4.05	

Is Scattering Important ?

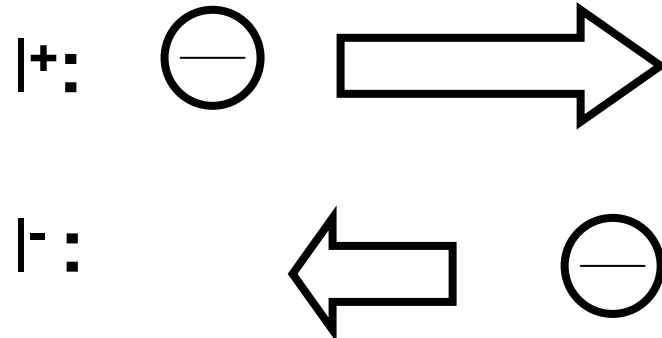
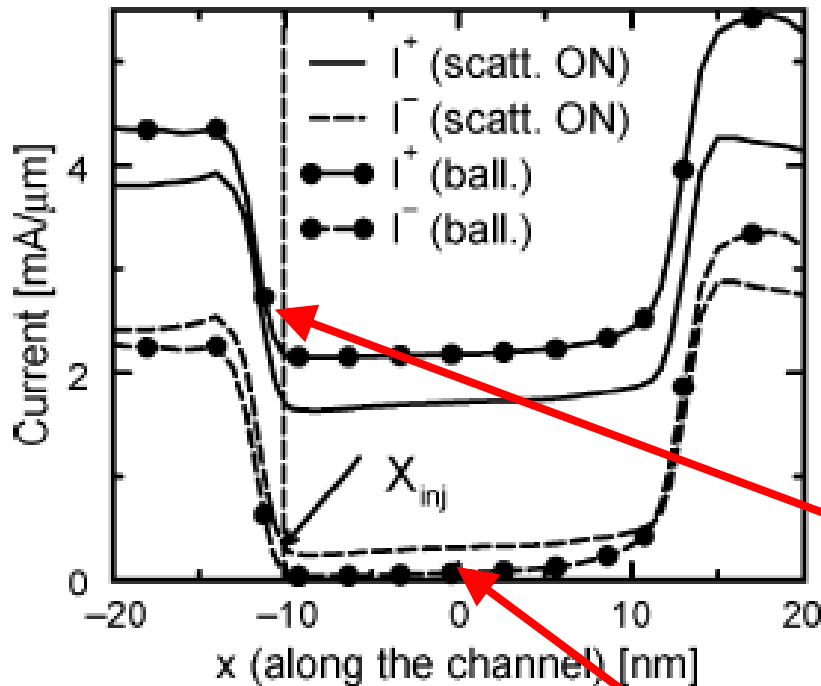


DG SOI $L_G = 25\text{nm}$
 $t_{OX} = 1.26\text{nm}$ $\epsilon_{OX} = 7$
 $t_{SI} = 10\text{nm}$ (45nm TN)

Ballistic:
no scattering
into the channel

Scattering affects I_{DS} !

Carrier fluxes inside the device

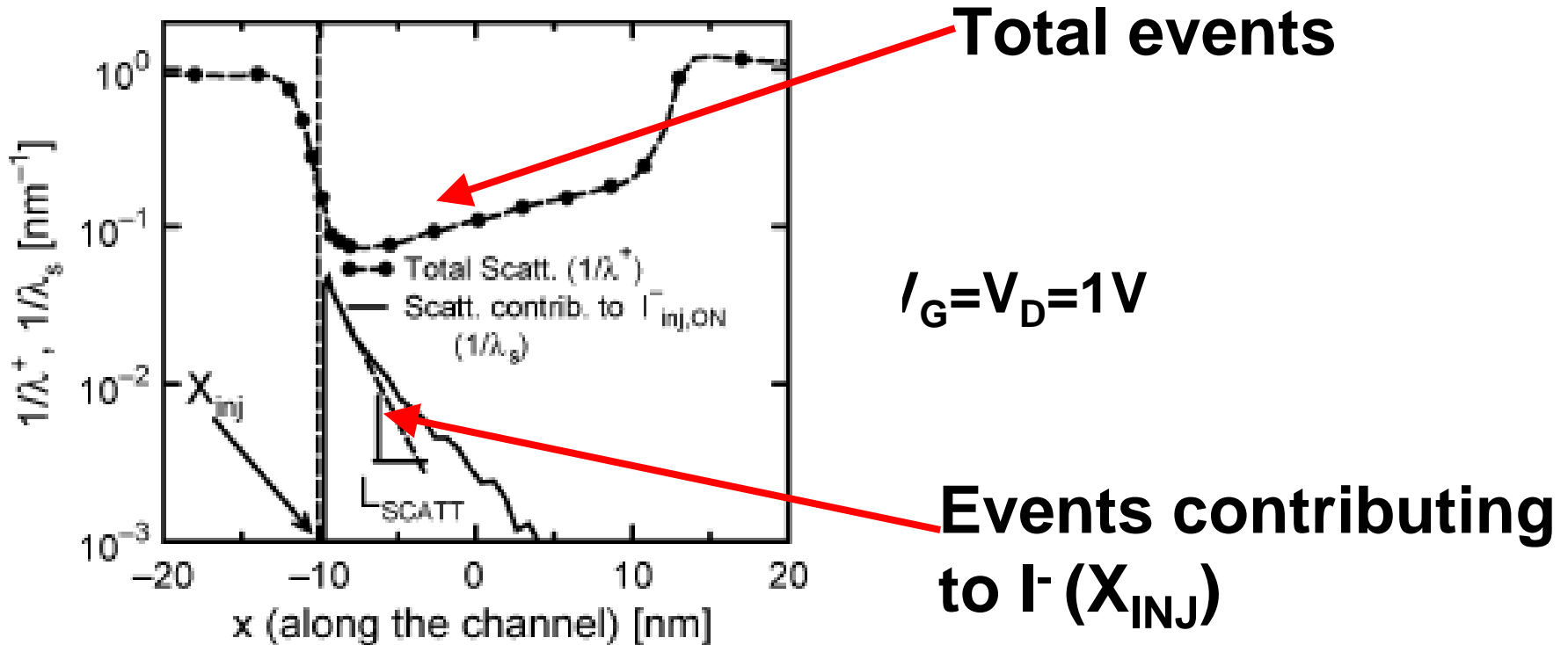


Virtual source

$$V_G = V_D = 1V$$

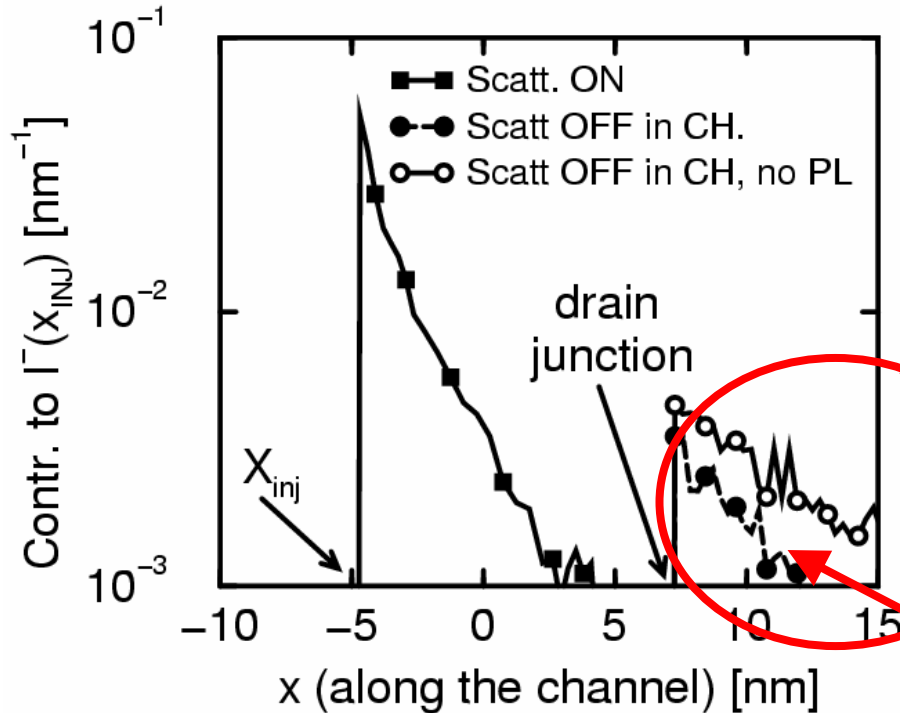
Presence of I^- inside the channel

Scattering contributing to $I^-(X_{INJ})$: where ?



**Only scattering events near
the virtual source contribute to $I^-(X_{INJ})$**

Back-Scattering at the drain

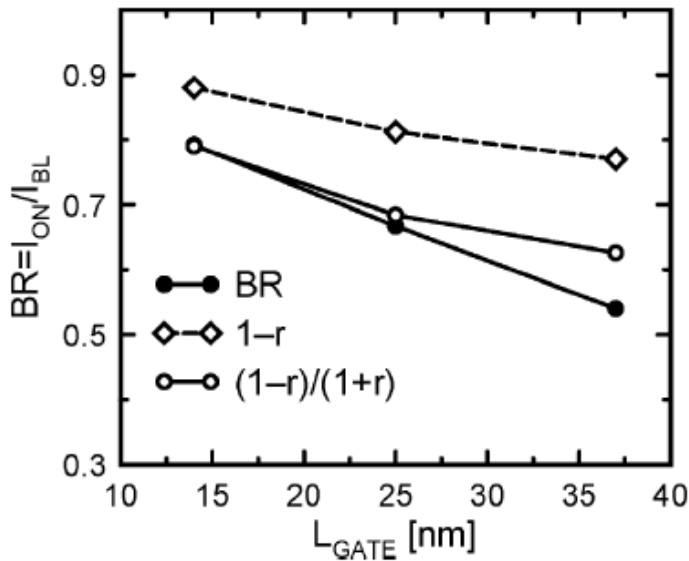


Back-scattering from the drain only when scattering in the channel is OFF

$V_G = V_D = 1\text{V}$
 $L_G = 14\text{nm}$

This effect is reduced when plasmons are present in the drain

Comparison with analytical model (Lundstrom EDL '97 and TED '02)

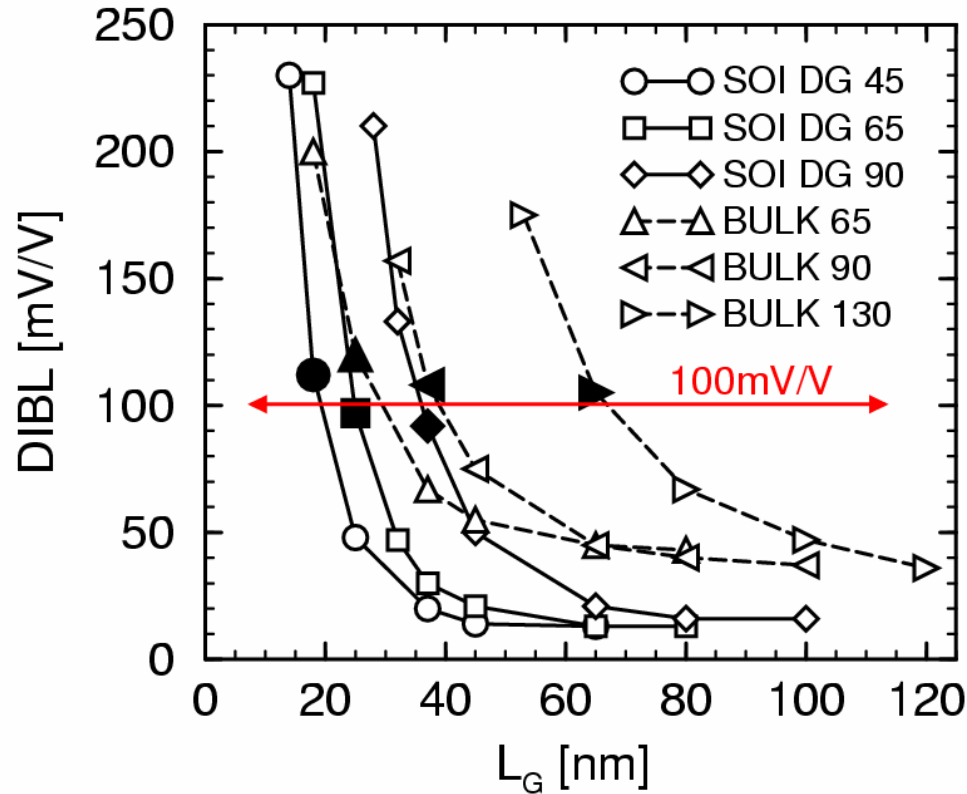


$$r = I^- (X_{INJ}) / I^+ (X_{INJ})$$

$$I_{ON} = I_{BL} (1-r) / (1+r)$$

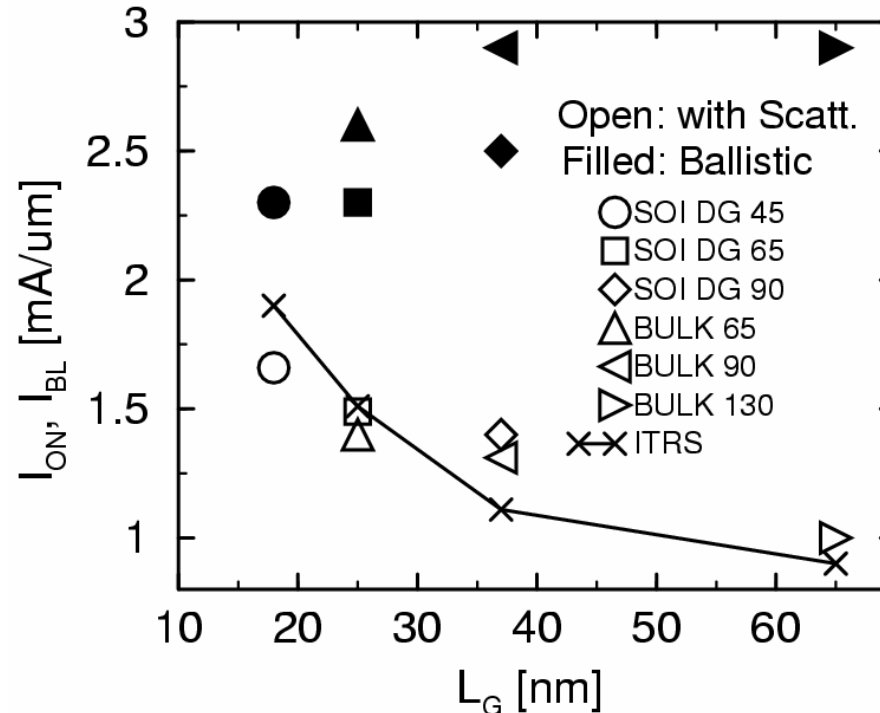
Analytical models cannot be used as postprocessors of ballistic simulations

Scaling and DIBL



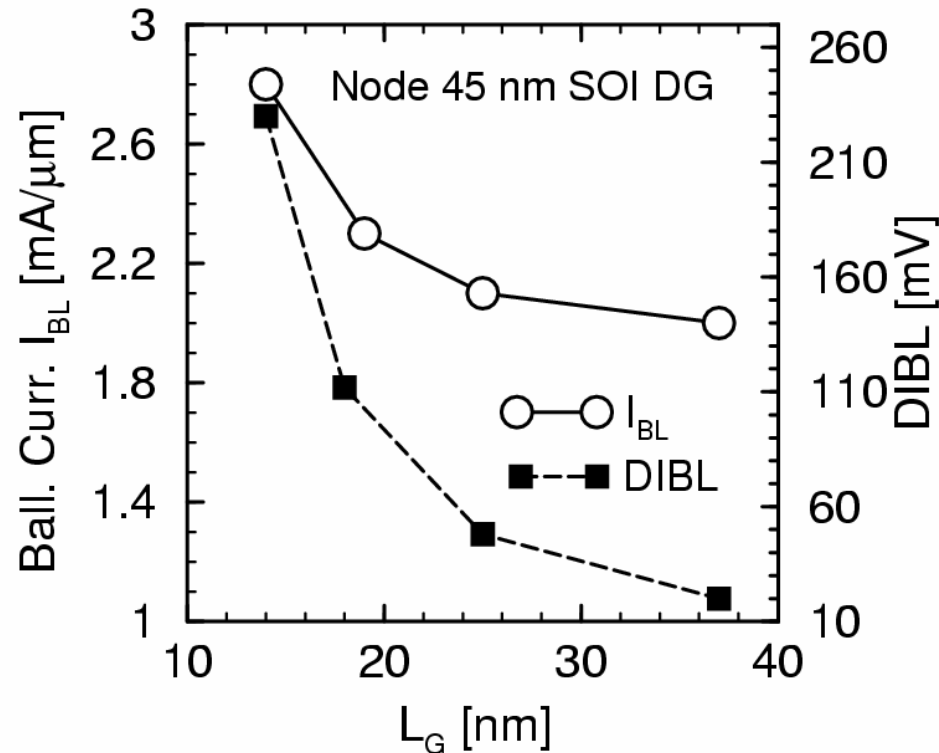
- All MOSFETs at nominal L_G of each TN:
DIBL \sim 100 [mV/V]

I_{BL} and I_{ON} at Nominal Gate Length (DIBL \sim [100mV/V])



- I_{BL} weakly depends on L_G at Nominal L_G
- N_{INV} at source roughly constant with L_G

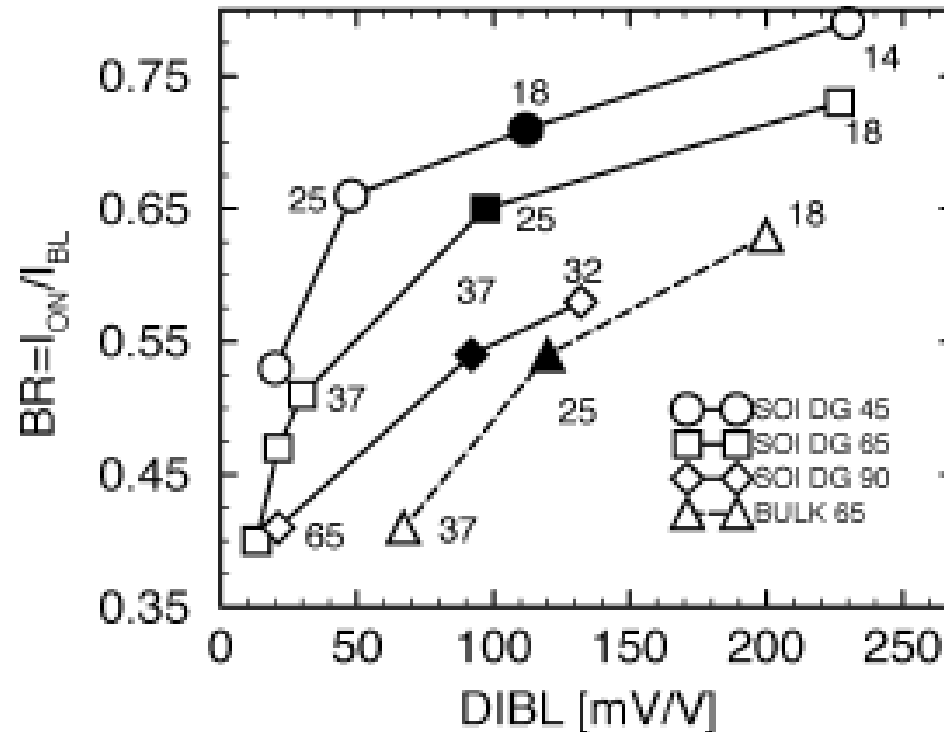
Ballistic Current and DIBL in a given TN



- Given a Technology Node the I_{BL} increases at small L_G together with DIBL:

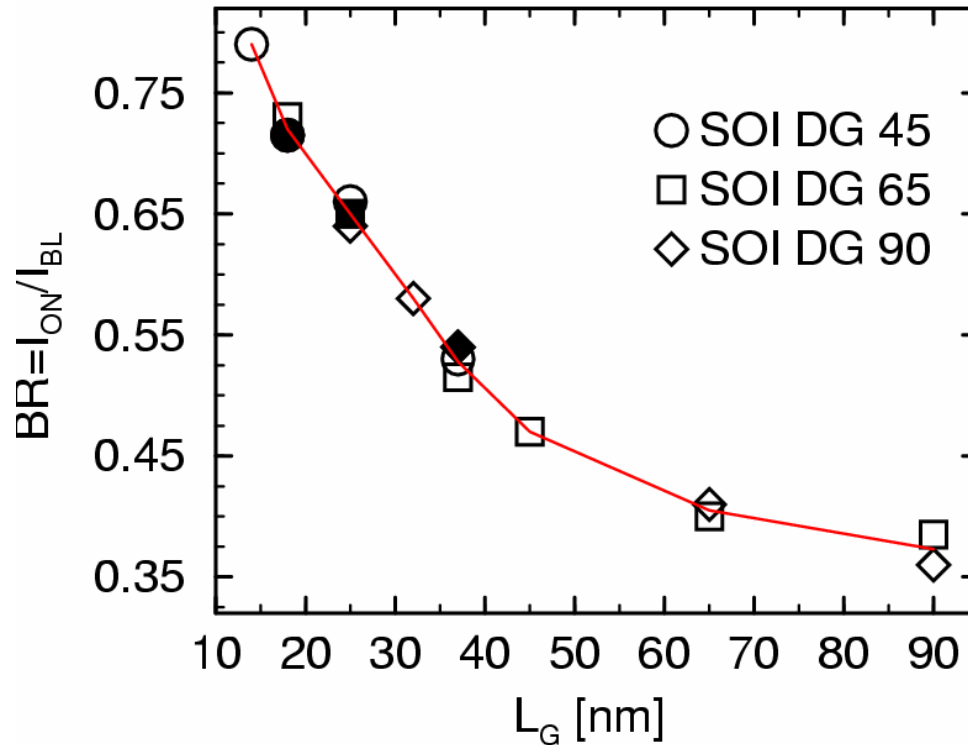
➔ Comparisons must be at a fixed DIBL

Ballistic Current and DIBL in a given TN



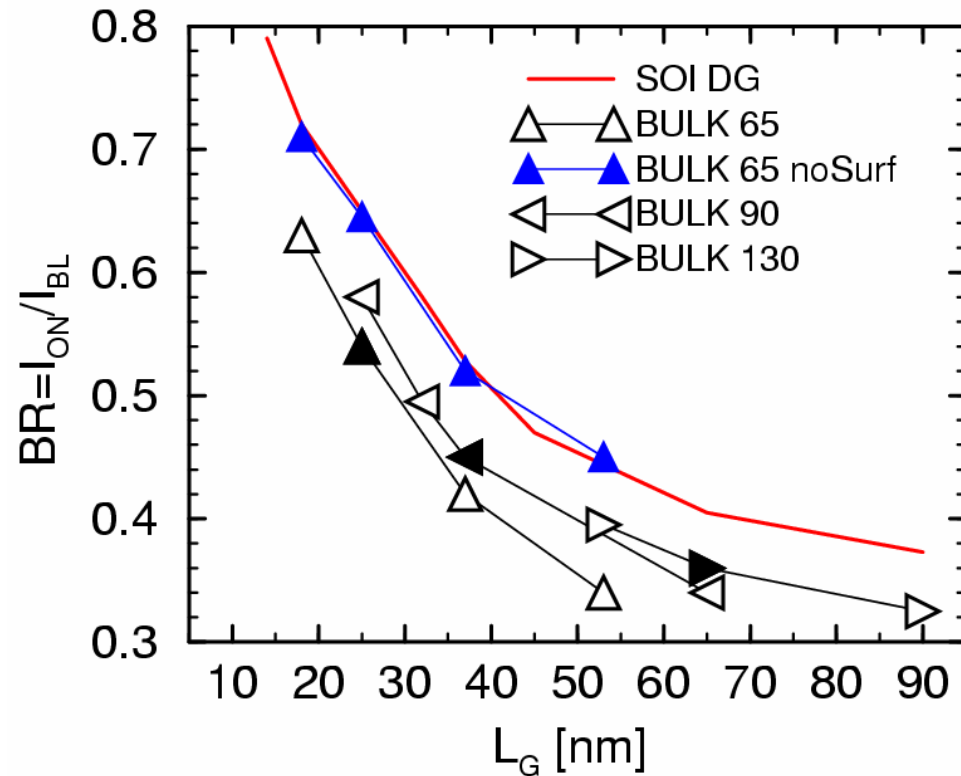
- BR can be increased by scaling at a cost of a larger DIBL
- SOI feature larger BR than Bulk

Ballistic Ratio for DG-SOI MOSFETs



- Universal Curve of BR vs. L_G for DG-SOI
- Depends on: Roadmap and device Architect.

Ballistic Ratio for Bulk and SOI MOSFETs



- Techn. Scaling increases E_{EFF} and Surf. Roughn. scattering in Bulk MOSFETs \rightarrow Degrades BR
- Surf. Roughn. OFF \rightarrow Back to DG-SOI Curve

Simulation Results

- Ballistic current I_{BL}
- On current I_{ON} (with scattering)
- Ballistic Ratio $BR = (I_{ON}/I_{BL})$



CONCLUSIONS (I)

- Low-field mobility in UT-SOI MOSFETS collapses at $T_{si} < 5$ nm.
- Scattering is still present in deca-nanometer MOSFETs, indicating that mobility partially maintains its role in determining I_{on} .
- The main role in reducing I_{ON} with respect to I_{BAL} is played by scattering events near the source barrier.



CONCLUSIONS (II)

- Improvements of BR with decreasing L_G in SOI MOSFETs indicate that “quasi-ballistic” transport is possible at L_G approx. 10-15 nm.
- In this quasi-ballistic transport regime I_{ON} will be determined more by the source injection velocity than by mobility, making UT silicon and UT strained silicon more appealing for future TN.



References for μ_{eff} Calculation

- Esseni et al., IEEE Transactions on ED , Vol. 50, Dec. 2003, pp. 2445 - 2455 (SOI mobility)
- Esseni et al., IEEE Transactions on ED, Vol. 51, March 2004, pp. 394 - 401 (surface roughness)
- Esseni et. al., IEEE Transactions on ED, Vol. 50, July 2003, pp. 1665 - 1674 (remote coulomb scattering)



References for μ_{eff} Calculation

- Esseni et al., IEEE Transactions on ED , Vol. 50, Dec. 2003, pp. 2445 - 2455 (SOI mobility)
- Esseni et al., IEEE Transactions on ED, Vol. 51, March 2004, pp. 394 - 401 (surface roughness)
- Esseni et. al., IEEE Transactions on ED, Vol. 50, July 2003, pp. 1665 - 1674 (remote coulomb scattering)



References for semi-ballistic transport in scaled MOSFETs

- P. Palestri et al., “Understanding Quasi-Ballistic Transport in Nano-MOSFETs: Part I—Scattering in the Channel and in the Drain”, TED-52, p. 2727, 2005
- S. Eminent et al., “...Part II—Technology Scaling Along the ITRS”, TED-52, p. 2736, 2005

