MosfetFab: Fabrication and characterization of MOS integrated devices

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Day 1 and 2: Clean-room work

The integrated electronic circuit technology has entered the nanotechnology and nanophysics era since deep-submicron metal oxide semiconductor field effect transistors (MOSFET) with 90nm channel length are already available in some modern electronic circuits. Upon the ongoing effort aimed at scaling down the MOSFET dimensions in order to enhance its performances in term of speed, power consumption and integration density, new physical phenomena are starting to come into play. Moreover, it is expected that in future devices, these phenomena, such as the quantum transport mechanisms, will strongly determine the physics of these devices. Interestingly, the key fabrication processes used in microelectronic devices in the past ten to twenty years are still in race in modern deep sub-micron technology. Of course, their performances have been continuously enhanced in order to allow the steady reduction of the device minimum feature size.

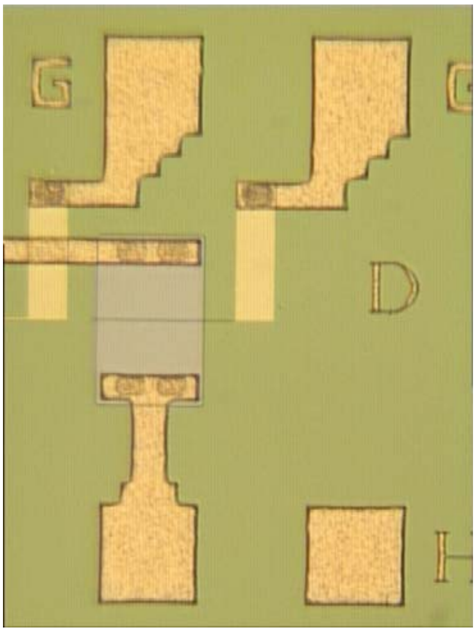

Fig. 1 : Optical microscope view of a n-MOS with 2 µm-wide poly-silicon gate fabricated by ESONN 2004 students. Fig. 2 : Mosfet electrical characterization practical at ESONN 2004.

In this practical, the key fabrication processes will be reviewed and used in the fabrication of a micron minimum feature size n-MOS test circuit comprising different integrated devices such as MOSFETs, MOS capacitors, inverters, diffused resistors, p-n diodes, …During the two days operation in clean rooms, the integrated test circuit will be fabricated starting from an almost virgin 2-inches silicon wafer. The n-MOSFETs have a self-aligned poly-silicon gate with a width down to 2 microns. The whole process includes the full set of usual clean-room fabrication and characterization techniques: wafer cleaning, multilevel UV lithography with mask alignment, thermal oxydation, thin film deposition by CVD and sputtering, ion implantation, chemical etching and reactive ion etching. The practical will offer the opportunity to discuss the physical mechanisms at work at every step.

The students will operate themselves the wafers during these different technological steps, so that they directly deal with the various physical and technical questions raised by the processes they operate. The resolution limit of UV lithography, the etch selectivity and directivity will be discussed. In-line physical characterization of wafers will include resistivity measurement and thickness measurements by both ellipsometry and surface profiling.

Day 3: Electrical characterization of integrated semiconductor devices

Device-level electrical test is a fundamental tool used for in-line and off-line monitoring of the integrated circuits manufacturing as well as in the research field on advanced integrated electronic devices. The main goal of this practical course is to get familiarized with the electrical test instrumental environment and with the test methodology of some of the main integrated devices, namely, the MOS capacitor, the diffused resistor, the n-type MOS field effect transistor (n-MOSFET) and the p-n diode. These tests will be conducted on the devices fabricated by the same group of students during the first two days. This makes possible a feedback on the fabrication process that usually reveals the impact of the process on the electrical characteristics.

More precisely, this course will show how physical (oxide thickness, doping…) as well as electrical parameters (threshold voltage, carrier mobility…) can be extracted from the device electrical characterization. Basic physical and electrical models will be applied to the analysis of the device characteristics. The behaviour of MOS capacitors in equilibrium, accumulation, depletion, and inversion regions is examined. We examine the capacitance-voltage characteristics of MOS capacitors from accumulation region to depletion region and study the effect of interfacial oxide charges on the MOS capacitor C-V characteristics. The n-MOSFET current-voltage characteristics will then be analysed in different bias conditions. Low-field carrier mobility in the inversion channel will be extracted using “long-channel” MOSFET models, and compared to the bulk value. The mobility roll-off observed at high electric field will then be characterized and modelled. The n-MOSFET sub-threshold current will be analysed in the light of the device electrical properties, in particular the density of surface states at the silicon-dielectric interface that can be extracted from the MOS capacitor analysis. It will be shown how this “leakage current” is detrimental for the static power consumption in the integrated circuits. Some short-channel effects in the MOSFET will then be pointed out such as the threshold voltage roll-off and current leakage. This will show why special measures must be taken to prevent these short-channel effects namely by following some "scaling rules" while scaling down MOSFETs geometry.