TP37 - Realisation and characterisation of nanowires Field Effect Transistor

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Over the past years, nanowires and nanotubes have attracted considerable interest due to their novel physical properties and diversity for potential electronic and photonic device applications [1, 2]. Two main approaches could be considered to fabricate nanowires. First, the top-down approach which uses advanced optical or electron-beam lithography in order to define and design the patterns, then followed by an etching process to obtain nanowires. In the bottom-up approach, nanowires are directly grown on a pre-patterned substrate from a metal catalyst using the chemical-vapour-deposition (CVD). These nanowires are then assembled to build devices. One of the crucial issues in the bottom-up approach is the positioning of the nanowires with respect to the other device features, such as contacts, to fabricate simple test structures to characterise their electronic properties. Many ways were used to integrate nanowires on electrical test structures.

For this practical work, we propose the realisation of a nanowires field effect transistor (FET) using photolithography [3] and/or electron beam lithography in order to connect the nanowires (figure 1) in the Plateforme Technologique Amont (PTA). Than we carried out the electrical characterisation of our SiNW FET using Keithley 4200 semiconductor characterization system at room temperature and in ambient

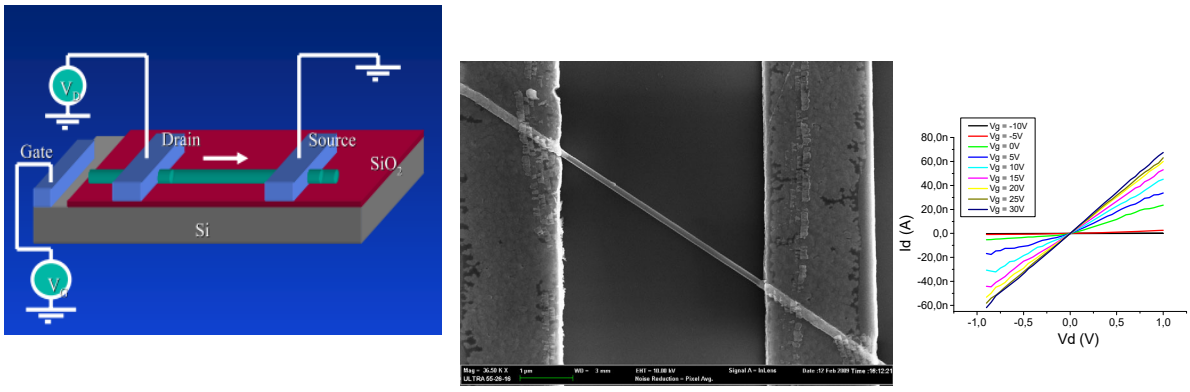

Figure 1: (a) Nanowire FET structure, (b) a typical SEM image of the nanowires of SiNW FET realized in the PTA and (c) the electrical characterisation of SiNW FET.

[1] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan and C. M. Lieber, Nature, 441, 489 (2006).
[2] Y. Huang, X. Duan and C. M. Lieber, Small, 1, 142 (2005).
[3] B. Salem et al. accepted in *Materials Science and Engineering: B (2008).*