19: Integrated circuit design using Magnetic Tunnel Junctions: from schematic to layout for analog and digital applications

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Among the non-volatile technologies considered today as a solution to contribute to push forward the incoming microelectronics limits, the MRAM technology (for Magnetic Random Access Memory) is one of the most promising, thanks to its combined advantages: it is intrinsically non-volatile, with a high writing speed (possibly close to SRAM memories), a low writing energy and a high density (possibly close to DRAM memories). Moreover, the basic elements of MRAM, the Magnetic Tunnel Junctions (MTJs) are immune to radiations, making it a good candidate for space applications.

Indeed, for more than 40 years, the microelectronics industry has been following the Moore's law, stating that the complexity and performance of microelectronics circuits should double every 18 months. However, this trend tends to get out of breath due to incoming physical limits. Indeed, the extreme miniaturization of the device results in a high power consumption mainly due to leakage currents, heating and reliability issues.

In order to be able to evaluate the gain that can be expected from combining MTJs with CMOS transistors for logic circuits, it is necessary to be able to integrate the magnetic devices in standard tools of microelectronics. The purpose of this practical work is to present the specific design tools and methods that have been developed, and use them to design a simple digital circuit made non-volatile by means of MTJs. Circuit level design of non-volatile memorization elements (Flip-Flop, registers) will be addressed (electrical simulations, layout, verifications), as well as the digital design of a simple logic circuit (digital simulation, logic synthesis, place and route)
The practical work will be based at the Centre Interuniversitaire de MicroElectronique (CIME) in Grenoble. No specific studies level is required to follow this practical work although basic notions of microelectronics design would be beneficial.

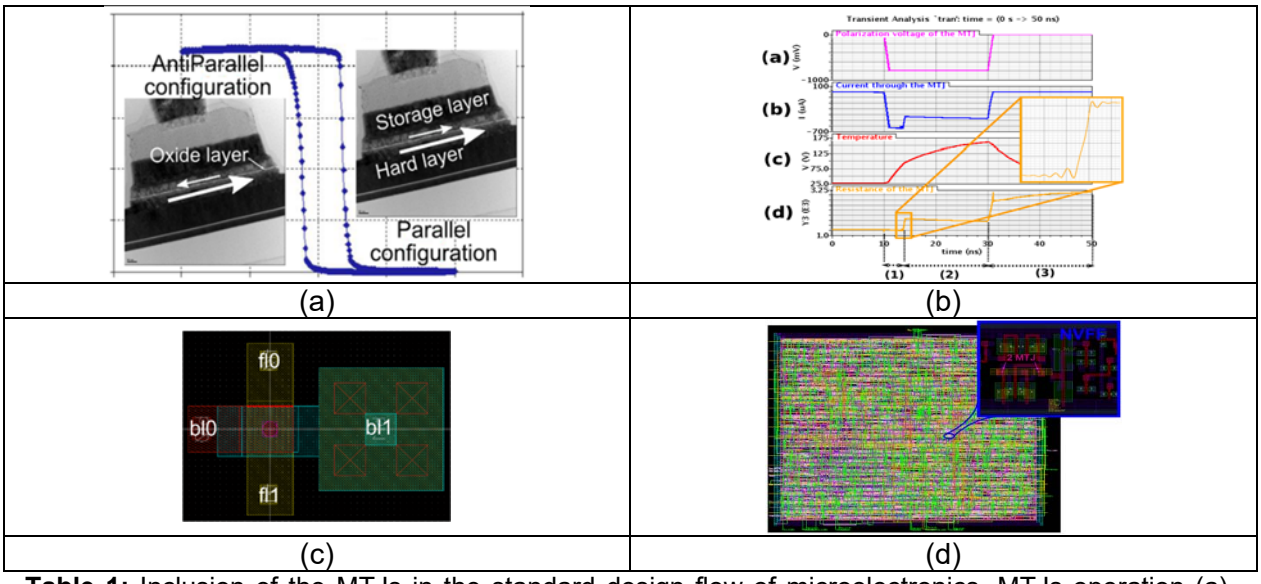

Table 1: Inclusion of the MTJs in the standard design flow of microelectronics. MTJs operation (a), electrical simulation using a compact model of the MTJ (b), pCell for layout implementation of an hybrid CMOS/magnetic circuit (c) and layout of a digital circuit made non-volatile by means of non-volatile Flip-Flops.

References: http://www.spintec.fr