CP3: Fabrication technologies and electrical characterization of semiconductor devices

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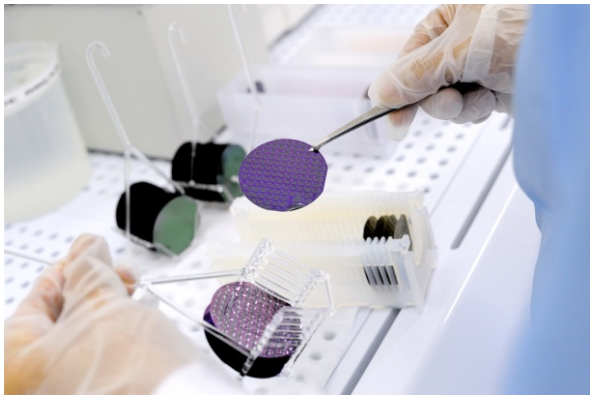
Day 1 and 2: Clean room facility

As the environment in the semiconductor industry scales down to nodes below 15 nm, more and more stringent requirements are being put on each technological process step involved in the overall fabrication process. As such, new materials, advanced deposition, etching and next generation lithography techniques are constantly evolving to reach enhanced performances in order to meet these scaling requirements.

In this two-day practical in the CIME Nanotech clean room facility, a group of 4 students will dedicate itself to the fabrication of four basic devices which are extensively used as building blocks in the design of integrated circuits: a PN diode, a MOS (Metal Oxide Semiconductor) capacitor, an n-MOS transistor and a Resistive RAM MIM (Metal Insulator Metal) structure. Current technological and physical issues raised at each up-to-date fabrication step will be addressed during the fulfillment of the process flow of each four basic devices.

Prior to fabrication, the overall process flow for each one of these devices will be presented and each key process step involved in standard production processes will be reviewed in detail. Technological operations devoted to handling procedures, wafer cleaning, oxide layer growth and control, shallow junction ion implantation, multi-level UV photolithography with mask alignment, thin film deposition by sputtering and Atomic Layer Deposition (ALD), and wet versus dry chemical etching will be provided.

Students themselves will manipulate the wafers at each technological step and operate the fabrication process flows under the supervision of a staff member, so that they can directly cope with problems raised by the process step at stake. This will provide an important hands-on experience in most significant technological steps involved in industrial manufacturing. In-line physical characterization of wafers will include resistivity and thickness measurements by both ellipsometry and surface profilometry along the process flows. A strong involvement of each student will be required to lead to efficient organization and cooperation within the group.



Day 3: Electrical characterization of integrated semiconductor devices

Device-level electrical test is a fundamental tool used for in-line and off-line monitoring of the integrated circuits manufacturing as well as in the research field on advanced integrated electronic devices. The main goal of this practical day is to get familiar with the electrical test instrumental environment and with the test methodology of a few integrated devices, namely the MOS capacitor, the diffused resistor, the n-type MOSFET and the p-n diode. These tests will be conducted on the devices that have been fabricated during the first two days spent in the clean room facility. This makes it possible to get a feedback on the fabrication process that usually reveals the impact of the process on the electrical characteristics.

More precisely, this course will show how physical properties (oxide thickness, doping concentration and depth…) and electrical parameters as well (threshold voltage, carrier mobility…) can be extracted from the device electrical behavior. Basic physical and electrical models will be applied to the analysis of the device electrical characteristics. The behavior of MOS capacitors in equilibrium, accumulation, depletion, and inversion regions will be examined. The capacitance-voltage characteristics of the MOS capacitors will be carried out from the accumulation regime to the depletion regime to study the effect of interfacial oxide charges on the MOS capacitor C(V) characteristics. The n-MOSFET current voltage characteristics will then be analyzed under several bias conditions. Low field carrier mobility in the inversion channel will be extracted using long-channel MOSFET models and compared to the bulk value. The mobility roll-off observed at high electric field will then be characterized and modeled. The n-MOSFET sub-threshold current will be discussed in the light of the device electrical properties; more specifically, information on the density of surface states at the silicon-dielectric interface can be extracted from the MOS capacitor analysis. It will be shown how this “leakage current” is detrimental for the static power consumption in integrated circuits. Some short-channel effects in the MOSFET will then be pointed out such as threshold voltage roll-off and current leakage. This will explain why special attention must be devoted to avoid these short-channel effects when following scaling down rules in the MOSFETs geometry.